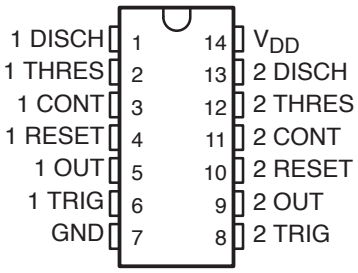
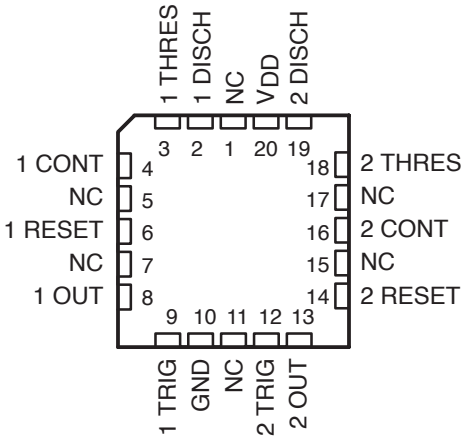
SLFS047B – FEBRUARY 1984 – REVISED SEPTEMBER 1997

- **Very Low Power Consumption . . . 2 mW Typ at V_{DD} = 5 V**
- **Capable of Operation in Astable Mode**
- **CMOS Output Capable of Swinging Rail to Rail**
- **High Output-Current Capability**
  Sink 100 mA Typ
  Source 10 mA Typ
- **Output Fully Compatible With CMOS, TTL, and MOS**
- **Low Supply Current Reduces Spikes During Output Transitions**
- **Single-Supply Operation From 2 V to 15 V**
- **Functionally interchangeable With the NE556; Has Same Pinout**

D, J, OR N PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC–No internal connection

description

The TLC556 series are monolithic timing circuits fabricated using the TI LinCMOS™ process, which provides full compatibility with CMOS, TTL, and MOS logic and operates at frequencies up to 2 MHz. Accurate time delays and oscillations are possible with smaller, less-expensive timing capacitors than the NE556 because of the high input impedance. Power consumption is low across the full range of power supply voltages.

Like the NE556, the TLC556 has a trigger level approximately one-third of the supply voltage and a threshold level approximately two-thirds of the supply voltage. These levels can be altered by use of the control voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset input can override all other inputs and can be used to initiate a new timing cycle. If the reset input is low, the flip-flop is reset and the output is low. Whenever the output is low, a low-impedance path is provided between the discharge terminal and ground.

While the CMOS output is capable of sinking over 100 mA and sourcing over 10 mA, the TLC556 exhibits greatly reduced supply-current spikes during output transitions. This minimizes the need for the large decoupling capacitors required by the NE556.

These devices have internal electrostatic-discharge (ESD) protection circuits that prevent catastrophic failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015. However, care should be exercised in handling these devices, as exposure to ESD may result in degradation of the device parametric performance.

All unused inputs should be tied to an appropriate logic level to prevent false triggering.

The TLC556C is characterized for operation from 0°C to 70°C. The TLC556I is characterized for operation from –40°C to 85°C. The TLC556M is characterized for operation over the full military temperature range of –55°C to 125°C.

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AVAILABLE OPTIONS

T_A RANGE	V_{DD} RANGE	PACKAGE				CHIP FORM (Y)
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	
O°C to 70°C	2 V to 18 V	TLC556CD			TLC556CN	TLC556Y
–4O°C to 85°C	3 V to 18 V	TLC556lD			TLC556IN	
–55°C to 125°C	5 V to 18 V	TLC556MD	TLC556MFK	TLC556MJ	TLC556MN	

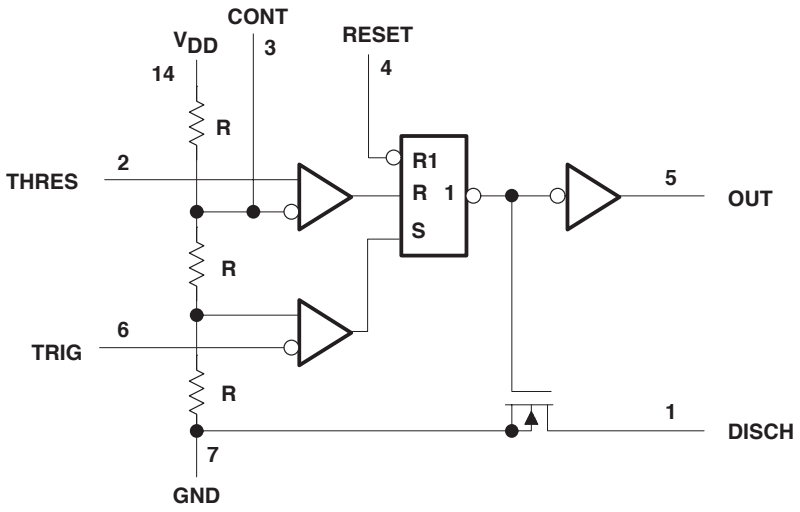
The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLC556CDR).

FUNCTION TABLE

RESET VOLTAGE†	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
< MIN	Irrelevant	Irrelevant	L	On
> MAX	< MIN	Irrelevant	H	Off
>MAX	>MAX	>MAX	L	On
> MAX	> MAX	< MIN	As previously established	

† For conditions shown as MIN or MAX, use the appropriate value specified under electrical characteristics.

functional block diagram (each timer)



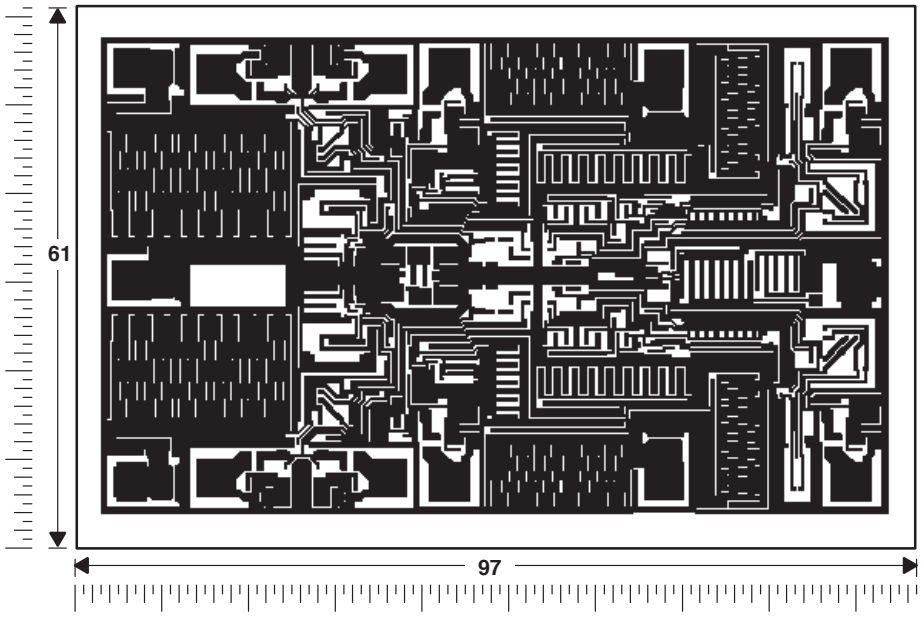
RESET can override TRIG and THRES.
TRIG can override THRES.

Pin numbers shown are for the D, J, or N packages.

TLC556Y chip information

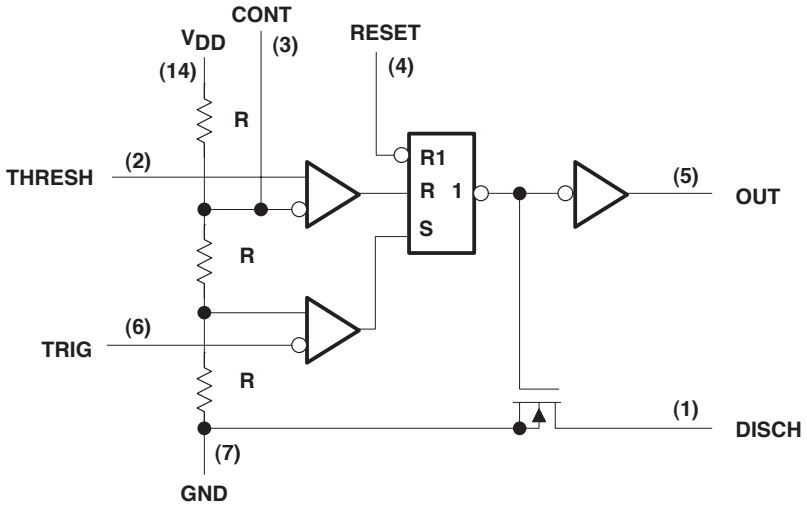
These chips, properly assembled, display characteristics similar to the TLC556 (see electrical table). Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS



CHIP THICKNESS: 15 TYPICAL
BONDING PADS: 4 × 4 MINIMUM
T_J max = 150°C
TOLERANCES ARE ±10%
ALL DIMENSIONS ARE IN MILS
NO BACKSIDE METALLIZATION
PIN (7) INTERNALLY CONNECTED TO BACKSIDE OF CHIP

FUNCTIONAL BLOCK DIAGRAM (EACH TIMER)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

		TLC556C	TLC556I	TLC556M	UNIT
Supply voltage, V_{DD} (see Note 1)		18	18	18	V
Input voltage range, V_I		−0.3 to V_{DD}	−0.3 to V_{DD}	−0.3 to V_{DD}	V
Sink current, discharge or output		150	150	150	mA
Source current, output		15	15	15	mA
Continuous total power dissipation		See Dissipation Rating Table			
Operating free-air temperature range		0 to 70	−40 to 85	−55 to 125	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package			260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J package			300	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or N package	260	260		

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	N/A
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	N/A

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2	15	V
Operating free-air temperature range, T_A	TLC556C	0	70	°C
	TLC556I	−40	85	
	TLC556M	−55	125	

electrical characteristics at specified free-air temperature, V_{DD} = 2 V for TLC556C, V_{DD} = 3 V for TLC556I

PARAMETER		TEST CONDITIONS	T_A†	TLC556C			TLC556I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IT}	Input threshold voltage		25°C	0.95	1.33	1.65	1.6	2	2.4	V
			Full range	0.85		1.75	1.5		2.5	
	Threshold current		25°C		10			10		pA
			MAX		75			150		
$V_{(trigger)}$	Trigger voltage		25°C	0.4	0.67	0.95	0.71	1	1.29	V
			Full range	0.3		1.05	0.61		1.39	
$I_{(trigger)}$	Trigger current		25°C		10			10		pA
			MAX		75			150		
$V_{(reset)}$	Reset voltage		25°C	0.4	1.1	1.5	0.4	1.1	1.5	V
			Full range	0.3		1.8	0.3		1.8	
$I_{(reset)}$	Reset current		25°C		10			10		pA
			MAX		75			150		
	Control voltage (open circuit) as a percentage of supply voltage		MAX		66.7%			66.7%		
	Discharge switch on-state voltage	I_{OL} = 1 mA	25°C		0.04	0.2		0.03	0.2	V
			Full range			0.25			0.375	
	Discharge switch off-state current		25°C		0.1			0.1		nA
			MAX		0.5			120		
V_{OH}	High-level output voltage	I_{OH} = –300 μA	25°C	1.5	1.9		1.5	1.9		V
			Full range	1.5			2.5			
V_{OL}	Low-level output voltage	I_{OL} = 1 mA	25°C		0.07	0.3		0.07	0.3	V
			Full range			0.35			0.4	
I_{DD}	Supply current	See Note 2	25°C		130	500		130	500	μA
			Full range			800			1000	

† Full range is 0°C to 70°C for TLC556C and –40°C to 85°C for TLC556I.

NOTE 2: These values apply for the expected operating configurations in which THRES is connected directly to DISCH or TRIG.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS	T_A†	TLC556C			TLC556I			TLC556M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IT}	Input threshold voltage		25°C	2.8	3.3	3.8	2.8	3.3	3.8	2.8	3.3	3.8	V
			Full range	2.7		3.9	2.7		3.9	2.7		3.9	
	Threshold current		25°C		10			10			10		pA
			MAX		75			150			5000		
$V_{(trigger)}$	Trigger voltage		25°C	1.36	1.66	1.96	1.36	1.66	1.96	1.36	1.66	1.96	V
			Full range	1.26		2.06	1.26		2.06	1.26		2.06	
$I_{(trigger)}$	Trigger current		25°C		10			10			10		pA
			MAX		75			150			5000		
$V_{(reset)}$	Reset voltage		25°C	0.4	1.1	1.5	0.4	1.1	1.5	0.4	1.1	1.5	V
			Full range	0.3		1.8	0.3		1.8	0.3		1.8	
$I_{(reset)}$	Reset current		25°C		10			10			10		pA
			MAX		75			150			5000		
	Control voltage (open circuit) as a percentage of supply voltage		MAX		66.7%			66.7%			66.7%		
	Discharge switch on-state voltage	I_{OL} = 10 mA	25°C		0.15	0.5		0.15	0.5		0.15	0.5	V
			Full range			0.6			0.6		0.6		
	Discharge switch off-state current		25°C		0.1			0.1			0.1		nA
			MAX		0.5			2			120		
V_{OH}	High-level output voltage	I_{OH} = –1 mA	25°C	4.1	4.8		4.1	4.8		4.1	4.8		V
			Full range	4.1			4.1			4.1			
V_{OL}	Low-level output voltage	I_{OL} = 8 mA	25°C		0.21	0.4		0.21	0.4		0.21	0.4	V
			Full range			0.5			0.5			0.6	
		I_{OL} = 5 mA	25°C		0.13	0.3		0.13	0.3		0.13	0.3	
			Full range			0.4			0.4			0.45	
		I_{OL} = 3.2 mA	25°C		0.08	0.3		0.08	0.3		0.08	0.3	
			Full range			0.35			0.35			0.4	
I_{DD}	Supply current	See Note 2	25°C		340	700		340	700		340	700	μA
			Full range			1000			1200			1400	

† Full range is 0°C to 70°C for TLC556C, –40°C to 85°C for TLC556I, and –55°C to 125°C for TLC556M.

NOTE 2: These values apply for the expected operating configurations in which THRES is connected directly to DISCH or to TRIG.

electrical characteristics at specified free-air temperature, V_{DD} = 15 V

PARAMETER		TEST CONDITIONS	T_A†	TLC556C			TLC556I			TLC556M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IT}	Input threshold voltage		25°C	9.45	10	10.55	9.45	10	10.55	9.45	10	10.55	V
			Full range	9.35		10.65	9.35		10.65	9.35		10.65	
	Threshold current		25°C		10			10			10		pA
			MAX		75			150			5000		
$V_{(trigger)}$	Trigger voltage		25°C	4.65	5	5.35	4.65	5	5.35	4.65	5	5.35	V
			Full range	4.55		5.45	4.55		5.45	4.55		5.45	
$I_{(trigger)}$	Trigger current		25°C		10			10			10		pA
			MAX		75			150			5000		
$V_{(reset)}$	Reset voltage		25°C	0.4	1.1	1.5	0.4	1.1	1.5	0.4	1.1	1.5	V
			Full range	0.3		1.8	0.3		1.8	0.3		1.8	
$I_{(reset)}$	Reset current		25°C		10			10			10		pA
			MAX		75			150			5000		
	Control voltage (open circuit) as a percentage of supply voltage		MAX		66.7%			66.7%			66.7%		
	Discharge switch on-state voltage	I_{OL} = 100 mA	25°C		0.8	1.7		0.8	1.7		0.8	1.7	V
			Full range			1.8			1.8			1.8	
	Discharge switch off-state current		25°C		0.1			0.1			0.1		nA
			MAX		0.5			2			120		
V_{OH}	High-level output voltage	I_{OH} = –10 mA	25°C	12.5	14.2		12.5	14.2		12.5	14.2		V
			Full range	12.5			12.5			12.5			
		I_{OH} = –5 mA	25°C	13.5	14.6		13.5	14.6		13.5	14.6		
			Full range	13.5			13.5			13.5			
		I_{OH} = –1 mA	25°C	14.2	14.9		14.2	14.9		14.2	14.9		
			Full range	14.2			14.2			14.2			
V_{OL}	Low-level output voltage	I_{OL} = 100 mA	25°C		1.28	3.2		1.28	3.2		1.28	3.2	V
			Full range			3.6			3.7			3.8	
		I_{OL} = 50 mA	25°C		0.63	1		0.63	1		0.63	1	
			Full range			1.3			1.4			1.5	
		I_{OL} = 10 mA	25°C		0.12	0.3		0.12	0.3		0.12	0.3	
			Full range			0.4			0.4			0.45	
I_{DD}	Supply current	See Note 2	25°C		0.72	1.2		0.72	1.2		0.72	1.2	mA
			Full range			1.6			1.8			2	

† Full range is 0°C to 70°C for TLC556C, –40°C to 85°C for TLC556I, and –55°C to 125°C for TLC556M.

NOTE 2: These values apply for the expected operating configurations in which THRES is connected directly to DISCH or TRIG.

electrical characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT}	Input threshold voltage		2.8	3.3	3.8	V
	Threshold current			10		pA
$V_{(trigger)}$	Trigger voltage		1.36	1.66	1.96	V
$I_{(trigger)}$	Trigger current			10		pA
$V_{(reset)}$	Reset voltage		0.4	1.1	1.5	V
$I_{(reset)}$	Reset current			10		pA
	Discharge switch on-state voltage	I_{OL} = 10 mA		0.15	0.5	V
	Discharge switch off-state current			0.1		nA
V_{OH}	High-level output voltage	I_{OH} = –1 mA	4.1	4.8		V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA		0.21	0.4	V
		I_{OL} = 5 mA		0.13	0.3	
		I_{OL} = 2.1 mA		0.08	0.3	
I_{DD}	Supply current	See Note 2		3.40	700	μA

NOTE 2: These values apply for the expected operating configurations in which THRES is connected directly to DISCH or TRIG.

operating characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Initial error of timing interval†	V_{DD} = 5 V to 15 V,	$R_A = R_B$ = 1 kΩ to 100 kΩ		1%	3%	
	Supply voltage sensitivity of timing interval	C_T = 0.1 μF,	See Note 3		0.1	0.5	%/V
t_r	Output pulse rise time	R_L = 10 MΩ,	C_L = 10 pF		20	75	ns
t_f	Output pulse fall time				15	60	
f_{max}	Maximum frequency in astable mode	R_A = 470 Ω, C_T = 200 pF,	R_B = 200 Ω, See Note 3	1.2	2.1		MHz

† Timing interval error is defined as the difference between the measured value and the average value of a random sample from each process run.

NOTE 3: R_A, R_B, and C_T are as defined in Figure 3.

TYPICAL CHARACTERISTICS

DISCHARGE SWITCH ON-STATE RESISTANCE vs FREE-AIR TEMPERATURE

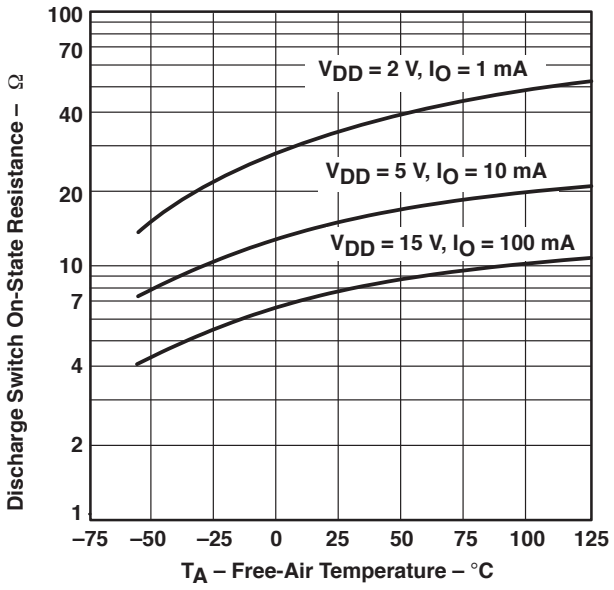
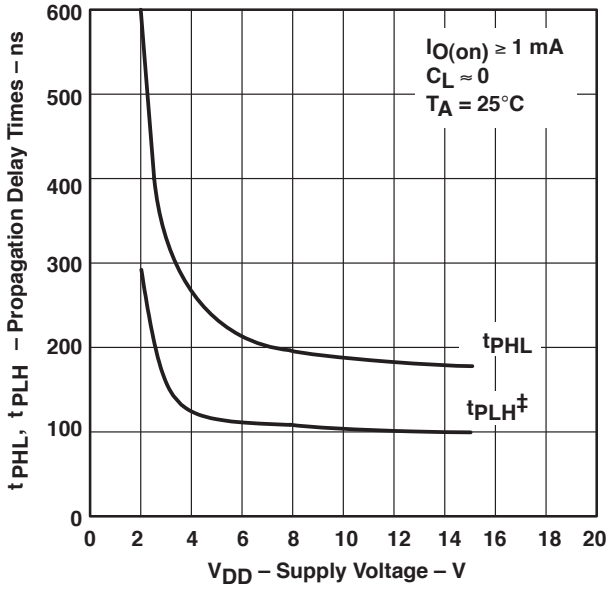


Figure 1

PROPAGATION DELAY TIMES (TO DISCHARGE OUTPUT FROM TRIGGER AND THRESHOLD SHORTED TOGETHER) vs SUPPLY VOLTAGE



‡ The effects of the load resistance on these values must be taken into account separately.

Figure 2

APPLICATION INFORMATION

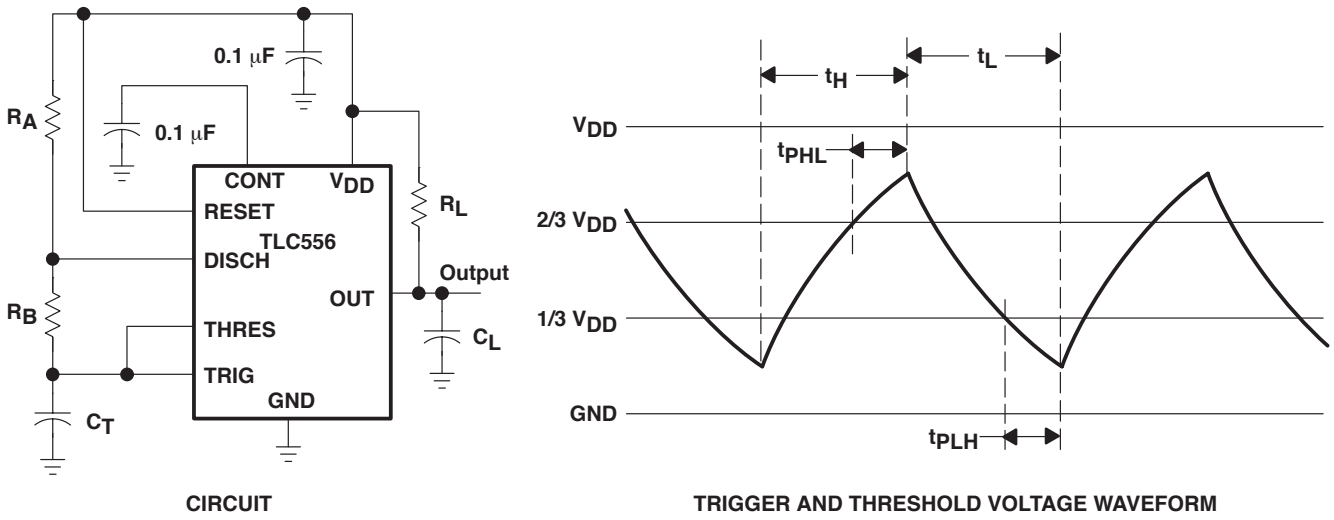


Figure 3. Astable Operation

Connecting the trigger input to the threshold input, as shown in Figure 3, causes the timer to run as a multivibrator. The capacitor C_T charges through R_A and R_B to the threshold voltage level (approximately 0.67 V_{DD}) and then discharges through R_B only to the value of the trigger voltage level (approximately 0.33 V_{DD}). The output is high during the charging cycle (t_H) and low during the discharge cycle (t_L). The duty cycle is controlled by the values of R_A, and R_B, and C_T, as shown in the equations below.

$$t_H \approx C_T (R_A + R_B) \ln 2 \quad (\ln 2 = 0.693)$$

$$t_L \approx C_T R_B \ln 2$$

$$\text{Period} = t_H + t_L \approx C_T (R_A + 2R_B) \ln 2$$

$$\text{Output driver duty cycle} = \frac{t_L}{t_H + t_L} \approx 1 - \frac{R_B}{R_A + 2R_B}$$

$$\text{Output waveform duty cycle} = \frac{t_H}{t_H + t_L} \approx \frac{R_B}{R_A + 2R_B}$$

The 0.1-μF capacitor at CONT in Figure 3 decreases the period by about 10%.

The formulas shown above do not allow for any propagation delay from the trigger and threshold inputs to the discharge output. These delay times add directly to the period and create differences between calculated and actual values that increase with frequency. In addition, the discharge output resistance r_{on} adds to R_B to provide another source of error in the calculation when R_B is very low or r_{on} is very high.

The equations below provide better agreement with measured values.

$$t_H = C_T (R_A + R_B) \ln \left[3 - \exp\left(\frac{-t_{PLH}}{C_T (R_B + r_{on})} \right) \right] + t_{PHL}$$

$$t_L = C_T (R_B + r_{on}) \ln \left[3 - \exp\left(\frac{-t_{PHL}}{C_T (R_A + R_B)} \right) \right] + t_{PLH}$$

APPLICATION INFORMATION

The preceding equations and those given earlier are similar in that a time constant is multiplied by the logarithm of a number or function. The limit values of the logarithmic terms must be between In 2 at low frequencies and In 3 at extremely high frequencies. For a duty cycle close to 50%, an appropriate constant for the logarithmic terms can be substituted with good results. Duty cycles less than 50% $\frac{t_H}{t_H + t_L}$ will require that $\frac{t_H}{t_L} < 1$ and possibly $R_A \leq r_{on}$. These conditions can be difficult to obtain.

In monostable applications, the trip point of the trigger input can be set by a voltage applied to CONT. An input voltage between 10% and 80% of the supply voltage from a resistor divider with at least 500-μA bias provides good results.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
5962-89503022A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-8950302CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
TLC556CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC556CDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC556CDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC556CDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC556CN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLC556CNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLC556ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC556IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC556IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC556IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC556IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLC556INE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLC556MD	ACTIVE	SOIC	D	14	50	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLC556MDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC556MDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC556MDRG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC556MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
TLC556MJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
TLC556MJB	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
TLC556MN	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements

for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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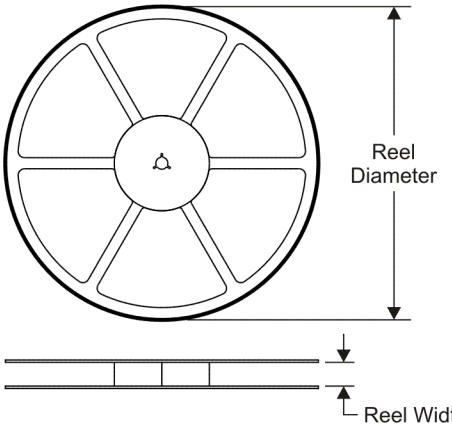
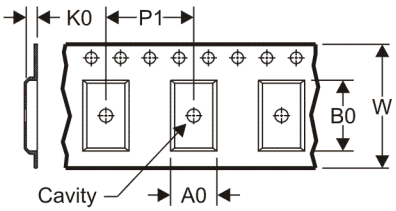
TAPE AND REEL INFORMATION

REEL DIMENSIONS

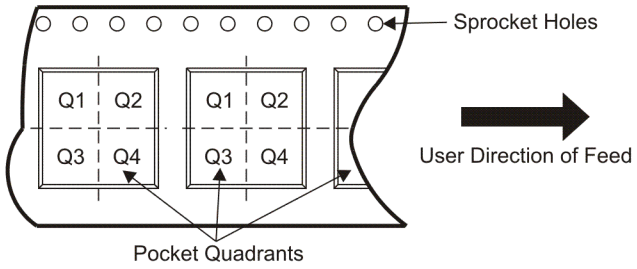


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

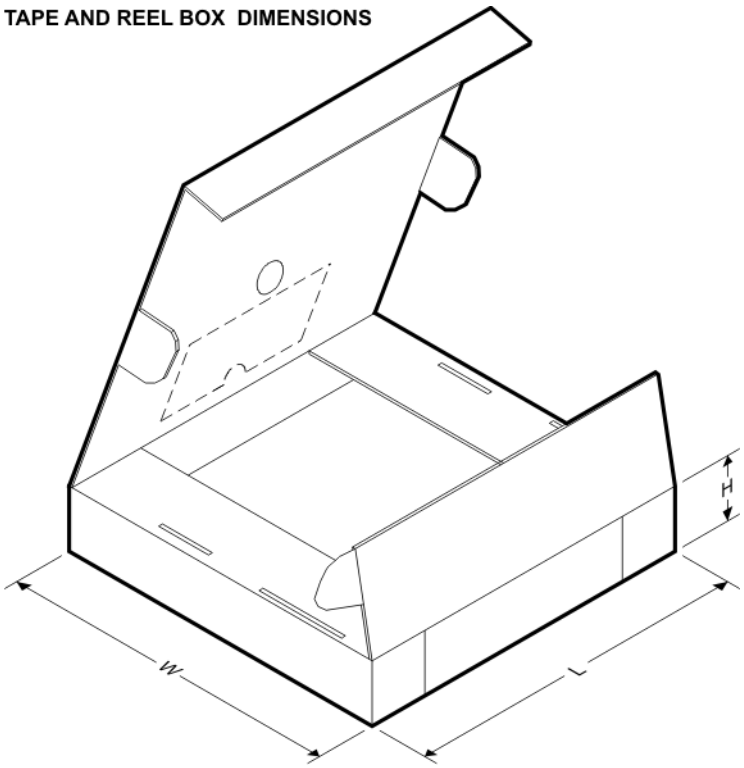
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC556CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC556IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



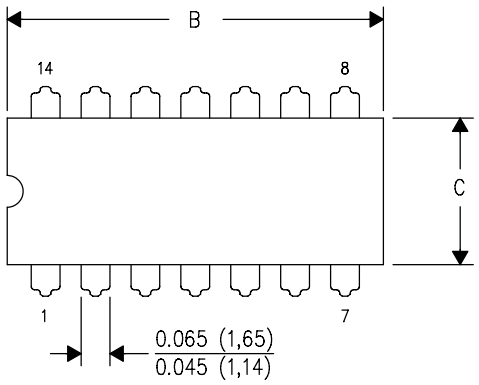
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC556CDR	SOIC	D	14	2500	333.2	345.9	28.6
TLC556IDR	SOIC	D	14	2500	346.0	346.0	33.0

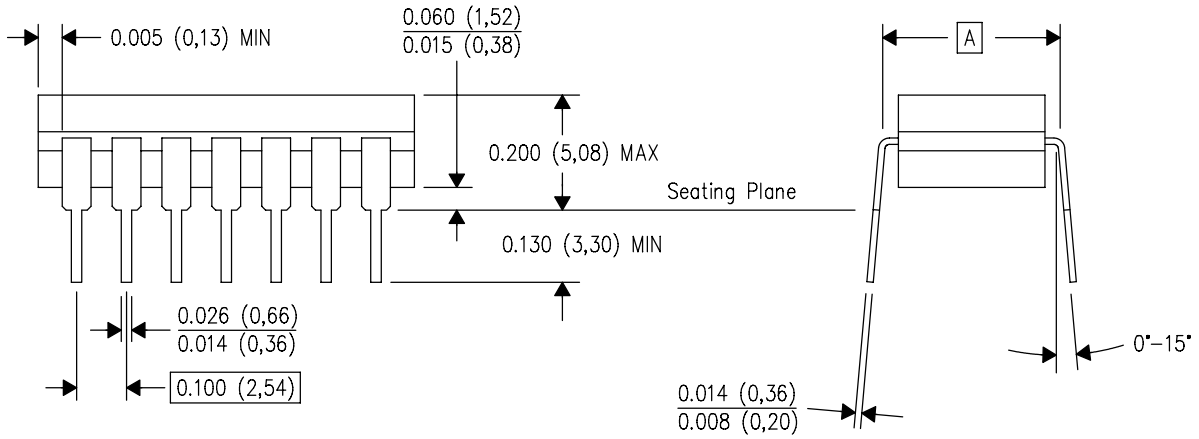
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

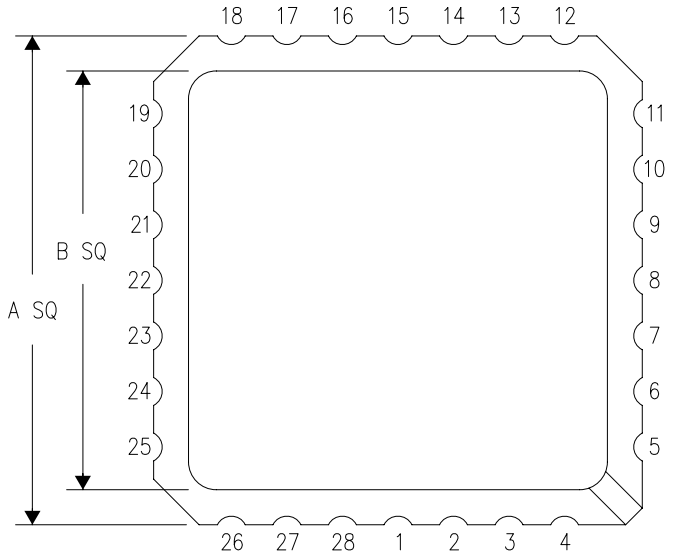


4040083/F 03/03

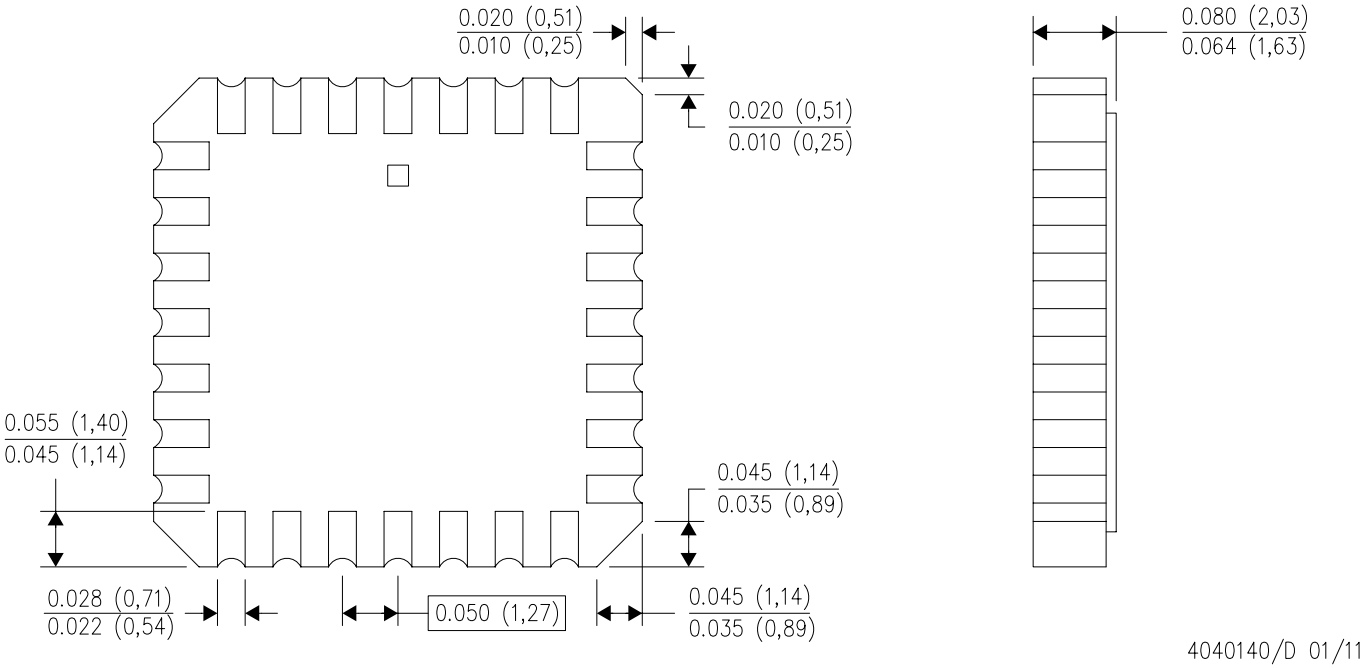
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



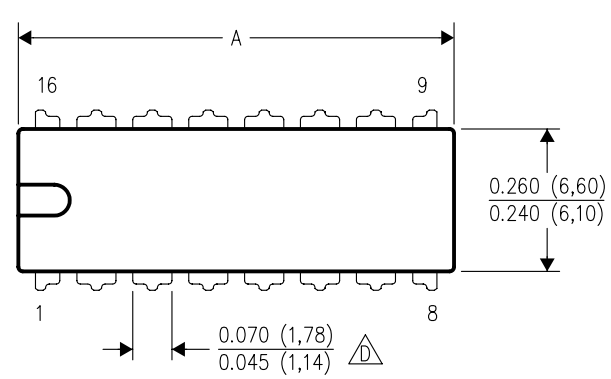
4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

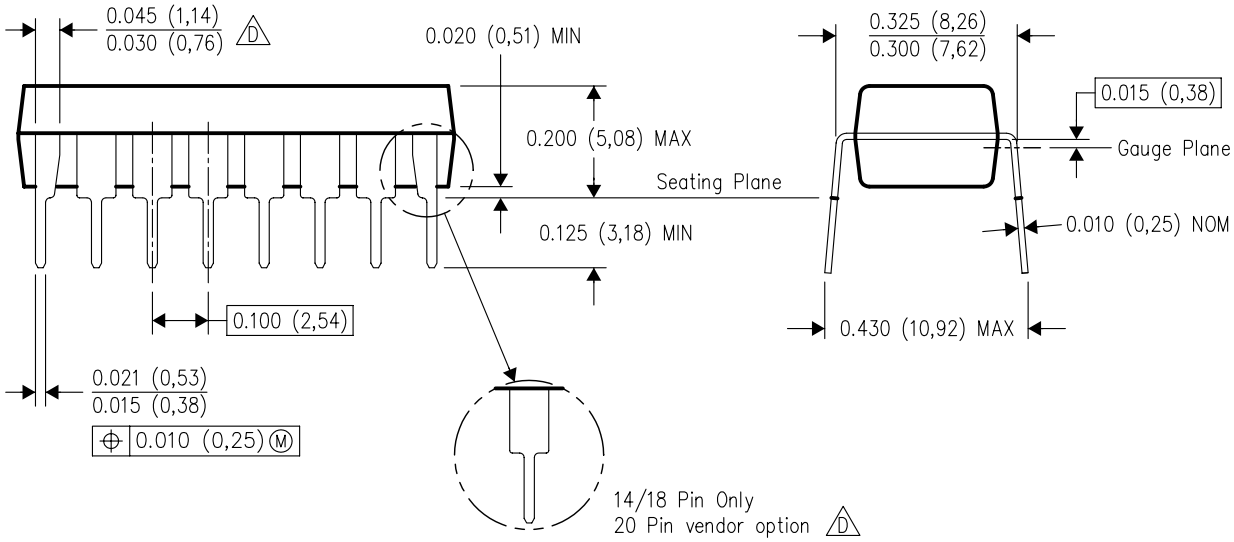
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



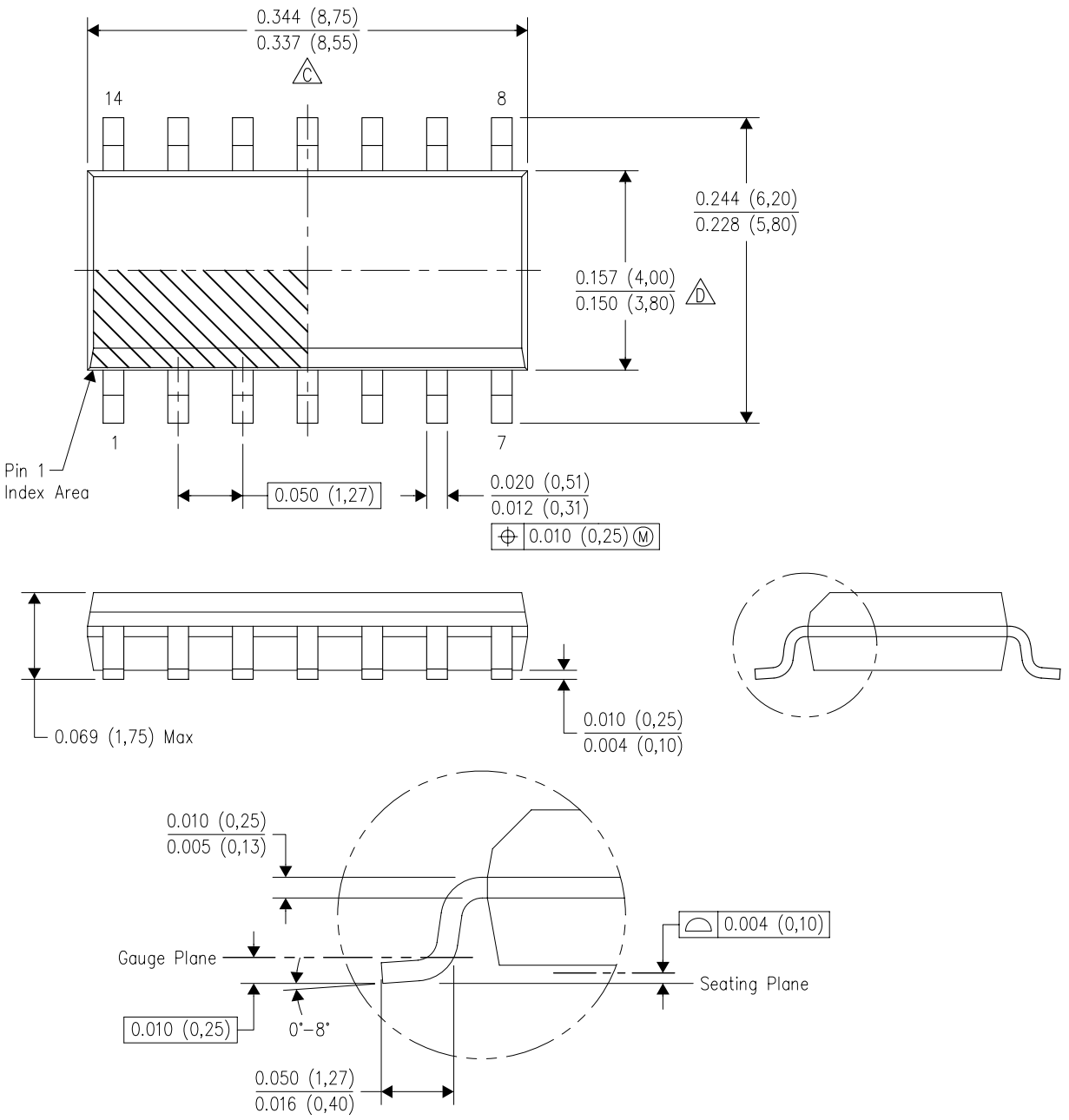
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

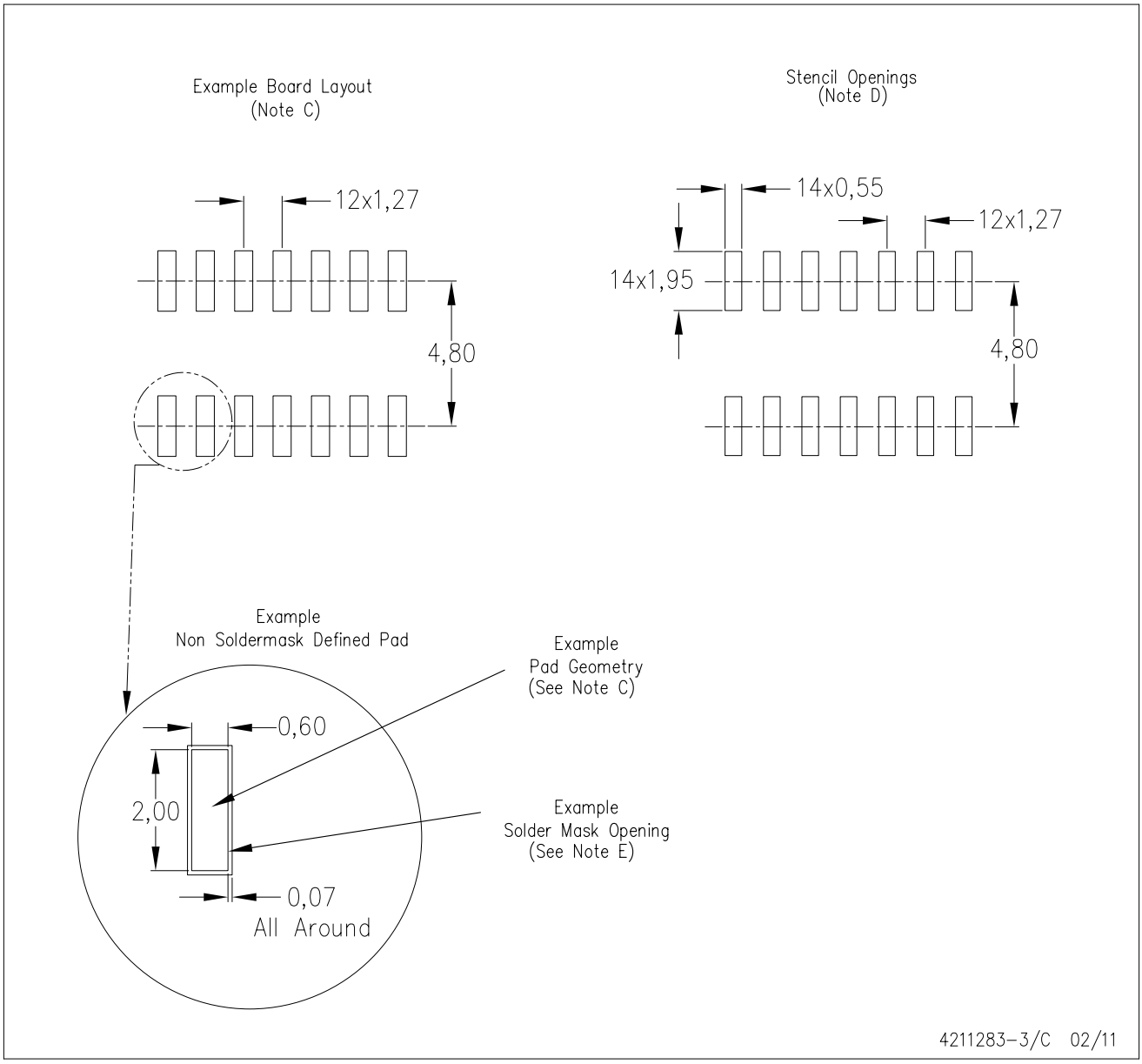
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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