Definitions of Ultra-Stable and Stable

Multilayer Ceramic Capacitors are generally divided into classes which are defined by the capacitance temperature characteristics over specified temperature ranges.

These are designated by alpha numeric codes.
Code definitions are summarised below and are also available in the relevant national and international specifications.

1. C0G/NP0 - Ultra Stable Class 1 Ceramic (EIA Class 1)

Spec.	Classification	Temperature range °C	Maximum capacitance change	Syfer dielectric code
CECC	1B/CG	-55 +125	0 ± 30ppm/°C	C
EIA	C0G/NP0	-55 +125	0 ± 30ppm/°C	C
MIL	CG (BP)	-55 +125	0 ± 30ppm/°C	C

Capacitors within this class have a dielectric constant range from 10 to 100. They are used in applications which require ultra stable dielectric characteristics with negligible dependence of capacitance and dissipation factor with time, voltage and frequency. They exhibit the following characteristics:-

a) Time does not significantly affect capacitance and dissipation factor (Tan δ) – no ageing.
b) Capacitance and dissipation factor are not affected by voltage.
c) Linear temperature coefficient.

2. X8R, X7R and X5R - Stable Class II Ceramic (EIA Class II)

Spec.	Classification	Temperature range °C	Maximum capacitance change % over temperature range		Syfer dielectric code
			No DC volt applied	Rated DC Volt	
CECC	2C1	-55 +125	±20	+20 -30	R
	2R1	-55 +125	±15	- -	X
	2X1	-55 +125	±15	+15 -25	B
EIA	X8R	-55 +150	±15	- -	N
	X7R	-55 +125	±15	- -	X
	X5R	-55 +85	±15	- -	P
MIL	BX	-55 +125	±15	+15 -25	B
	BZ	-55 +125	±20	+20 -30	R

Capacitors of this type have a dielectric constant range of 1000-4000, and also have a non-linear temperature characteristic which exhibits a dielectric constant variation of less than ±15% (2R1) from its room temperature value, over the specified temperature range. Generally used for by-passing (decoupling), coupling, filtering, frequency discrimination, DC blocking and voltage transient suppression with greater volumetric efficiency than Class I units, whilst maintaining stability within defined limits.

Capacitance and dissipation factor are affected by:-
Time (Ageing)
Voltage (AC or DC)
Frequency

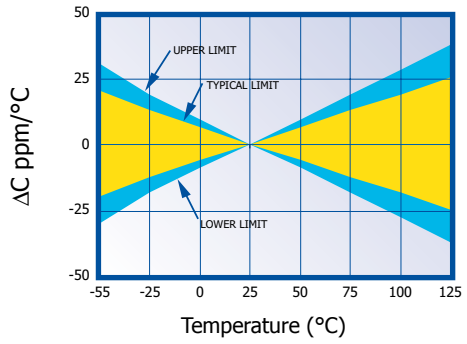
3. Technical Summary

	C0G/NP0			X8R	X7R			X5R
Dielectric characteristics	Ultra stable			Stable	Stable			Stable
IECQ-CECC	1B/CG	-	-	-	2C1	2R1	2X1	-
EIA	-	C0G/NP0	-	X8R	-	X7R	-	X5R
MIL	-	-	CG (BP)	-	BZ	-	BX	-
Rated temperature range	-55ºC to +125ºC			-55ºC to +150ºC	-55ºC to +125ºC			-55ºC to +85ºC
Maximum capacitance change over temperature range								
No DC voltage applied	0 ± 30 ppm/ºC			± 15%	± 20%	± 15%	± 15%	± 15%
Rated DC voltage applied				-	+20 -30%	-	+15 -25%	-
Syfer dielectric ordering code	C			N	R	X	B	P
Tangent of loss angle (tan δ)	Cr > 50pF ≤ 0.0015 Cr ≤ 50pF = 0.0015 $(\frac{15}{Cr} + 0.7)$			≤ 0.025	≤ 0.025			≤ 0.025

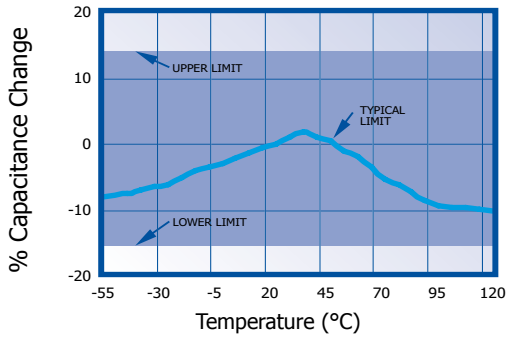
The table above highlights the difference in coding for IECQ-CECC, EIA and MIL standards when defining the temperature coeffiecient and the voltage coefficient.

	C0G/NP0	X8R	X7R	X5R
Insulation resistance (Ri) Time constant (Ri x Cr) (whichever is the least)	100G Ω or 1000s	100G Ω or 1000s	100G Ω or 1000s	100G Ω or 1000s
Capacitance tolerance	Cr < 10pF ± 0.05pF (H) ± 0.10pF (B) ± 0.25pF (C) ± 0.50pF (D) Cr ¸ 10pF ± 1.0pF (F) ± 1% (F) ± 2% (G) ± 5% (J) ± 10% (K)	± 5% (J) ± 10% (K) ± 20% (M)	± 5% (J) ± 10% (K) ± 20% (M)	± 5% (J) ± 10% (K) ± 20% (M)
Dielectric strength	**Voltage applied for 5 seconds. Charging current limited to 50 mA maximum.**			
16-200V ⩾200V 500V 500V/630V >1kV 4-6kV	2.5 times Rated voltage + 250V 1.5 times 1.5 times 1.2 times	2.5 times	2.5 times Rated voltage + 250V 1.5 times 1.25 times 1.2 times	2.5 times
Climatic category (IEC)				
Chip	55/125/56	55/150/56	55/125/56	55/85/56
Dipped	55/125/21	-	55/125/21	-
Discoidal	55/125/56	-	55/125/56	-
Ageing characteristic (Typical)	Zero	1% per time decade	1% per time decade	1% per time decade
Approvals				
Chip	QC-32100	-	QC-32100	-
Dipped radial	IECQ-CECC 30601-008	-	IECQ-CECC 30701-013	-

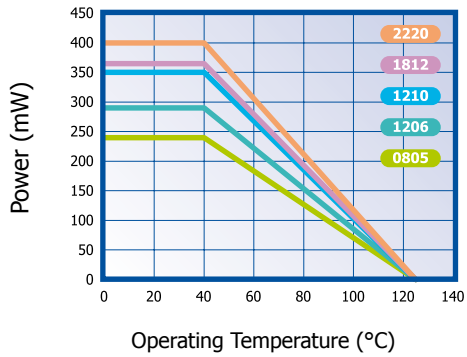
Typical dielectric temperature characteristics C0G/NP0 capacitance vs temperature



X7R capacitance vs temperature

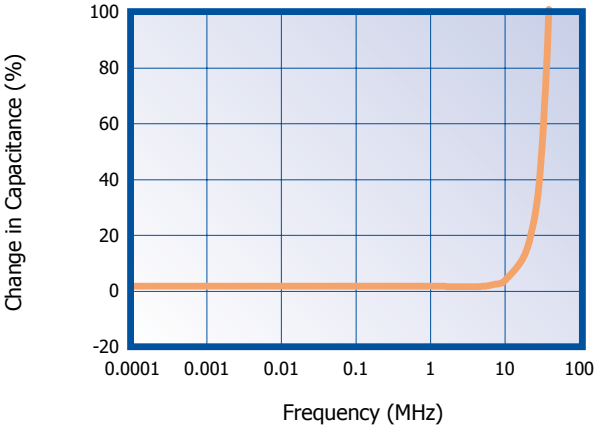


Power ratings for C0G/NP0 and X7R



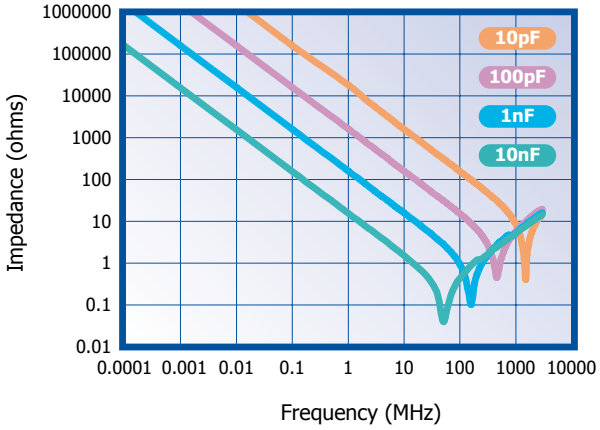
Capacitance vs Frequency - 10nF chip

Ultra Stable C0G dielectric

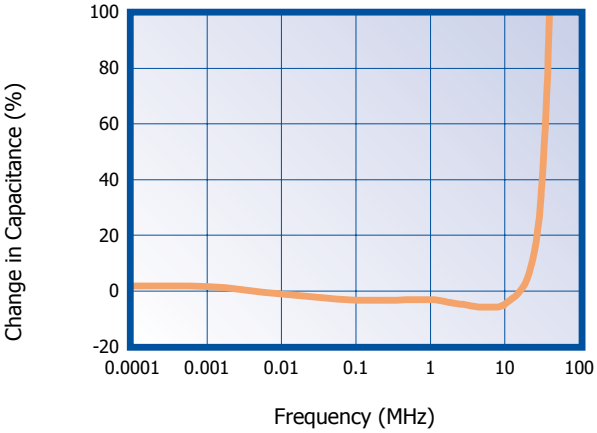


Impedance vs Frequency - chips

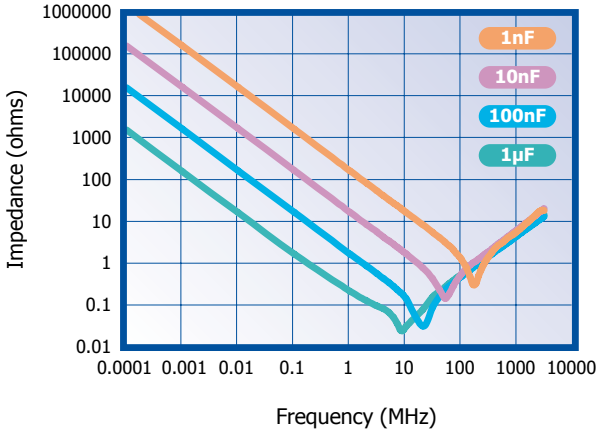
Ultra Stable C0G dielectric



Stable X7R dielectric

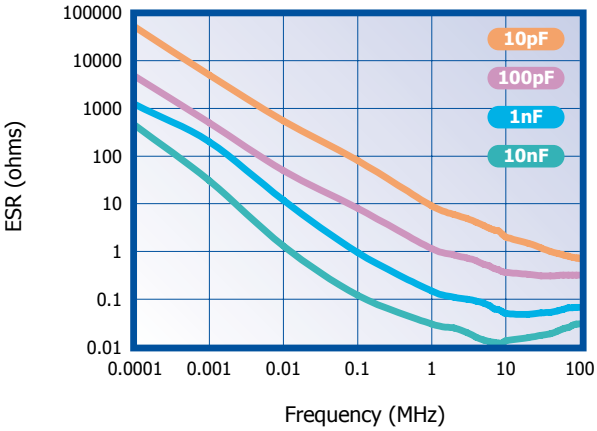


Stable X7R dielectric

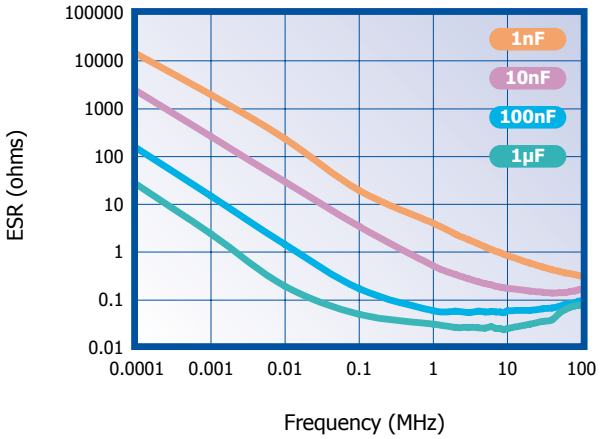


E.S.R. vs Frequency - chips

Ultra Stable C0G dielectric



Stable X7R dielectric



Ageing

Capacitor ageing is a term used to describe the negative, logarithmic capacitance change which takes place in ceramic capacitors with time. The crystalline structure for barium titanate based ceramics changes on passing through its Curie temperature (known as the Curie Point) at about 125°C. This domain structure relaxes with time and in doing so, the dielectric constant reduces logarithmically; this is known as the ageing mechanism of the dielectric constant. The more stable dielectrics have the lowest ageing rates.

The ageing process is reversible and repeatable. Whenever the capacitor is heated to a temperature above the Curie Point the ageing process starts again from zero.

The ageing constant, or ageing rate, is defined as the percentage loss of capacitance due to the ageing process of the dielectric which occurs during a decade of time (a tenfold increase in age) and is expressed as percent per logarithmic decade of hours. As the law of decrease of capacitance is logarithmic, this means that in a capacitor with an ageing rate of 1% per decade of time, the capacitance will decrease at a rate of:

a) 1% between 1 and 10 hours
b) An additional 1% between the following 10 and 100 hours
c) An additional 1% between the following 100 and 1000 hours
d) An additional 1% between the following 1000 and 10000 hours etc
e) The ageing rate continues in this manner throughout the capacitor's life.

Typical values of the ageing constant for our Multilayer Ceramic Capacitors are:

Dielectric class	Typical agreed value
Ultra Stable C0G/NP0	Negligible capacitance loss through ageing
Stable X7R	1% per decade of time

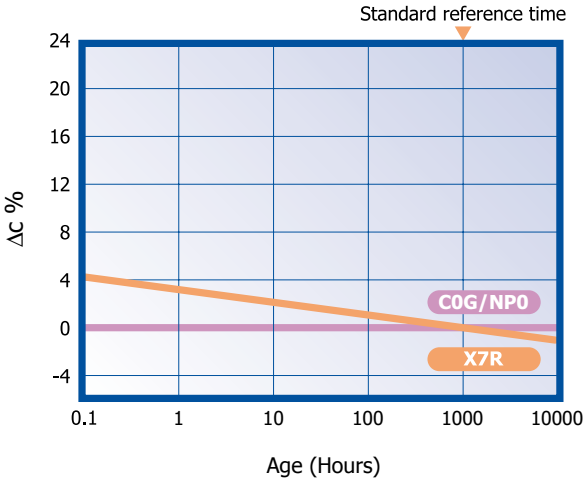
Capacitance measurements

Because of ageing it is necessary to specify an age for reference measurements at which the capacitance shall be within the prescribed tolerance. This is fixed at 1000 hours, since for practical purposes there is not much further loss of capacitance after this time.

All capacitors shipped are within their specified tolerance at the standard reference age of 1000 hours after having cooled through their Curie temperature.

The ageing curve for any ceramic dielectric is a straight line when plotted on semi-log paper.

Capacitance vs time - Ageing



Summary and conclusions

1.0 The recommended sequence of testing Multilayer Ceramic Capacitors is as follows:

a) Capacitance. Applying factors based on the manufacturer's ageing rate and the time elapsed since the last Curie temperature excursion.

b) Dissipation factor

c) Voltage proof test

d) Insulation resistance

e) Other tests. If any limits are specified for change in capacitance during a long term test (life test, for example), the capacitor should be de-aged before both initial and final measurements. De-ageing is accomplished by exposure of the capacitors to 150°C for 1 hour (without voltage) and stabilised at room temperature for 24 hours before capacitance measurements are made.

2.0 The ageing process is completely repeatable and predictable for a given capacitor.

3.0 Capacitance change is negative and logarithmic in respect to time.

4.0 Class C0G/NP0 dielectric has a negligible ageing rate.

5.0 Class 2 ceramic dielectrics have ageing rates which will be typically 1% for X8R, X7R and X5R but up to 8% for other dielectrics dependent upon particular ceramic composition employed. This wide capacitance change, as a result of 'shelf' ageing and temperature cycling, illustrates why close-tolerance (less than ±5%) high dielectric constant ceramics should not be specified.

6.0 Soldering both leaded and chip class 2 capacitors into a circuit will, because of the ageing phenomenon, give a temporary increase in capacitance value. The magnitude of this change will be dependent on the soldering temperature, time and dielectric class.