

DATA SHEET

NE/SA/SE555/SE555C Timer

Product data
Supersedes data of 1994 Aug 31

2003 Feb 14

Timer

NE/SA/SE555/SE555C

DESCRIPTION

The 555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200 mA.

FEATURES

- Turn-off time less than 2 μ s
- Max. operating frequency greater than 500 kHz
- Timing from microseconds to hours
- Operates in both astable and monostable modes
- High output current
- Adjustable duty cycle
- TTL compatible
- Temperature stability of 0.005% per $^{\circ}$ C

APPLICATIONS

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation

PIN CONFIGURATION

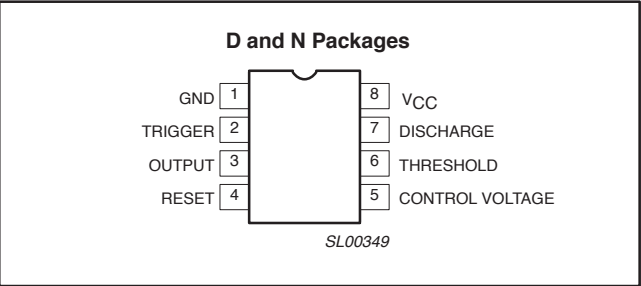


Figure 1. Pin configuration

BLOCK DIAGRAM

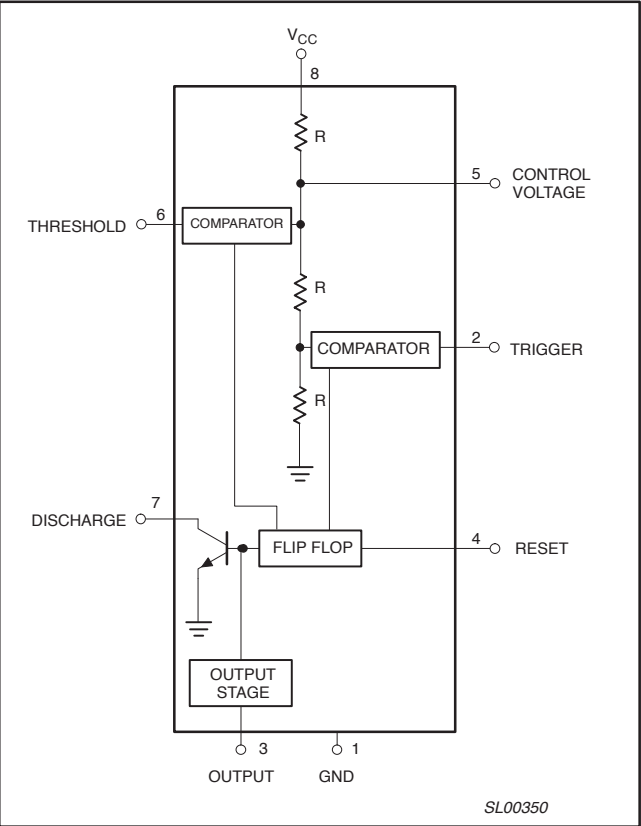


Figure 2. Block Diagram

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Small Outline (SO) Package	0 to +70 $^{\circ}$ C	NE555D	SOT96-1
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70 $^{\circ}$ C	NE555N	SOT97-1
8-Pin Plastic Small Outline (SO) Package	-40 $^{\circ}$ C to +85 $^{\circ}$ C	SA555D	SOT96-1
8-Pin Plastic Dual In-Line Package (DIP)	-40 $^{\circ}$ C to +85 $^{\circ}$ C	SA555N	SOT97-1
8-Pin Plastic Dual In-Line Package (DIP)	-55 $^{\circ}$ C to +125 $^{\circ}$ C	SE555CN	SOT97-1
8-Pin Plastic Dual In-Line Package (DIP)	-55 $^{\circ}$ C to +125 $^{\circ}$ C	SE555N	SOT97-1

Timer

NE/SA/SE555/SE555C

EQUIVALENT SCHEMATIC

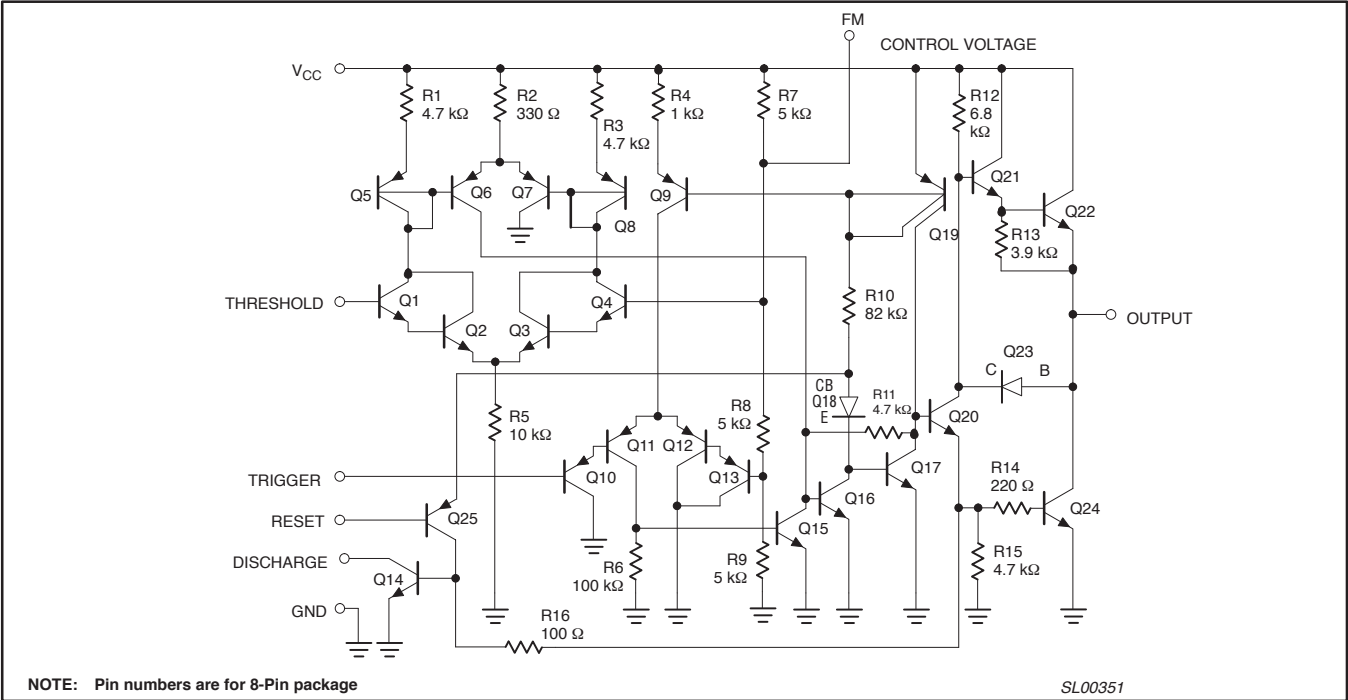


Figure 3. Equivalent schematic

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V _{CC}	Supply voltage		
	SE555	+18	V
	NE555, SE555C, SA555	+16	V
P _D	Maximum allowable power dissipation ¹	600	mW
T _{amb}	Operating ambient temperature range		
	NE555	0 to +70	°C
	SA555	−40 to +85	°C
	SE555, SE555C	−55 to +125	°C
T _{stg}	Storage temperature range	−65 to +150	°C
T _{SOLD}	Lead soldering temperature (10 sec max)	+230	°C

NOTE:

1. The junction temperature must be kept below 125 °C for the D package and below 150 °C for the N package.
At ambient temperatures above 25 °C, where this limit would be derated by the following factors:
D package 160 °C/W
N package 100 °C/W

Timer

NE/SA/SE555/SE555C

DC AND AC ELECTRICAL CHARACTERISTICS

T_{amb} = 25 °C, V_{CC} = +5 V to +15 V unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE555			NE555/SA555/SE555C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	Supply voltage		4.5		18	4.5		16	V
I _{CC}	Supply current (low state) ¹	V _{CC} = 5 V, R _L = ∞ V _{CC} = 15 V, R _L = ∞		3 10	5 12		3 10	6 15	mA mA
t _M Δt _M /ΔT Δt _M /ΔV _S	Timing error (monostable) Initial accuracy ² Drift with temperature Drift with supply voltage	R _A = 2 kΩ to 100 kΩ C = 0.1 μF		0.5 30 0.05	2.0 100 0.2		1.0 50 0.1	3.0 150 0.5	% ppm/°C %/V
t _A Δt _A /ΔT Δt _A /ΔV _S	Timing error (astable) Initial accuracy ² Drift with temperature Drift with supply voltage	R _A , R _B = 1 kΩ to 100 kΩ C = 0.1 μF V _{CC} = 15 V		4 0.15	6 500 0.6		5 0.3	13 500 1	% ppm/°C %/V
V _C	Control voltage level	V _{CC} = 15 V V _{CC} = 5 V	9.6 2.9	10.0 3.33	10.4 3.8	9.0 2.6	10.0 3.33	11.0 4.0	V V
V _{TH}	Threshold voltage	V _{CC} = 15 V V _{CC} = 5 V	9.4 2.7	10.0 3.33	10.6 4.0	8.8 2.4	10.0 3.33	11.2 4.2	V V
I _{TH}	Threshold current ³			0.1	0.25		0.1	0.25	μA
V _{TRIG}	Trigger voltage	V _{CC} = 15 V V _{CC} = 5 V	4.8 1.45	5.0 1.67	5.2 1.9	4.5 1.1	5.0 1.67	5.6 2.2	V V
I _{TRIG}	Trigger current	V _{TRIG} = 0 V		0.5	0.9		0.5	2.0	μA
V _{RESET}	Reset voltage ⁴	V _{CC} = 15 V, V _{TH} = 10.5 V	0.3		1.0	0.3		1.0	V
I _{RESET}	Reset current Reset current	V _{RESET} = 0.4 V V _{RESET} = 0 V		0.1 0.4	0.4 1.0		0.1 0.4	0.4 1.5	mA mA
V _{OL}	LOW-level output voltage	V _{CC} = 15 V I _{SINK} = 10 mA I _{SINK} = 50 mA I _{SINK} = 100 mA I _{SINK} = 200 mA		0.1 0.4 2.0 2.5	0.15 0.5 2.2		0.1 0.4 2.0 2.5	0.25 0.75 2.5	V V V V
		V _{CC} = 5 V I _{SINK} = 8 mA I _{SINK} = 5 mA		0.1 0.05	0.25 0.2		0.3 0.25	0.4 0.35	V V
V _{OH}	HIGH-level output voltage	V _{CC} = 15 V I _{SOURCE} = 200 mA I _{SOURCE} = 100 mA		12.5 13.0			12.5 13.3		V V
		V _{CC} = 5 V I _{SOURCE} = 100 mA	3.0	3.3		2.75	3.3		V
t _{OFF}	Turn-off time ⁵	V _{RESET} = V _{CC}		0.5	2.0		0.5	2.0	μs
t _R	Rise time of output			100	200		100	300	ns
t _F	Fall time of output			100	200		100	300	ns
	Discharge leakage current			20	100		20	100	nA

NOTES:

- Supply current when output high typically 1 mA less.
- Tested at V_{CC} = 5 V and V_{CC} = 15 V.
- This will determine the max value of R_A+R_B, for 15 V operation, the max total R = 10 MΩ, and for 5 V operation, the max. total R = 3.4 MΩ.
- Specified with trigger input HIGH.
- Time measured from a positive-going input pulse from 0 to 0.8×V_{CC} into the threshold to the drop from HIGH to LOW of the output. Trigger is tied to threshold.

Timer

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TYPICAL PERFORMANCE CHARACTERISTICS

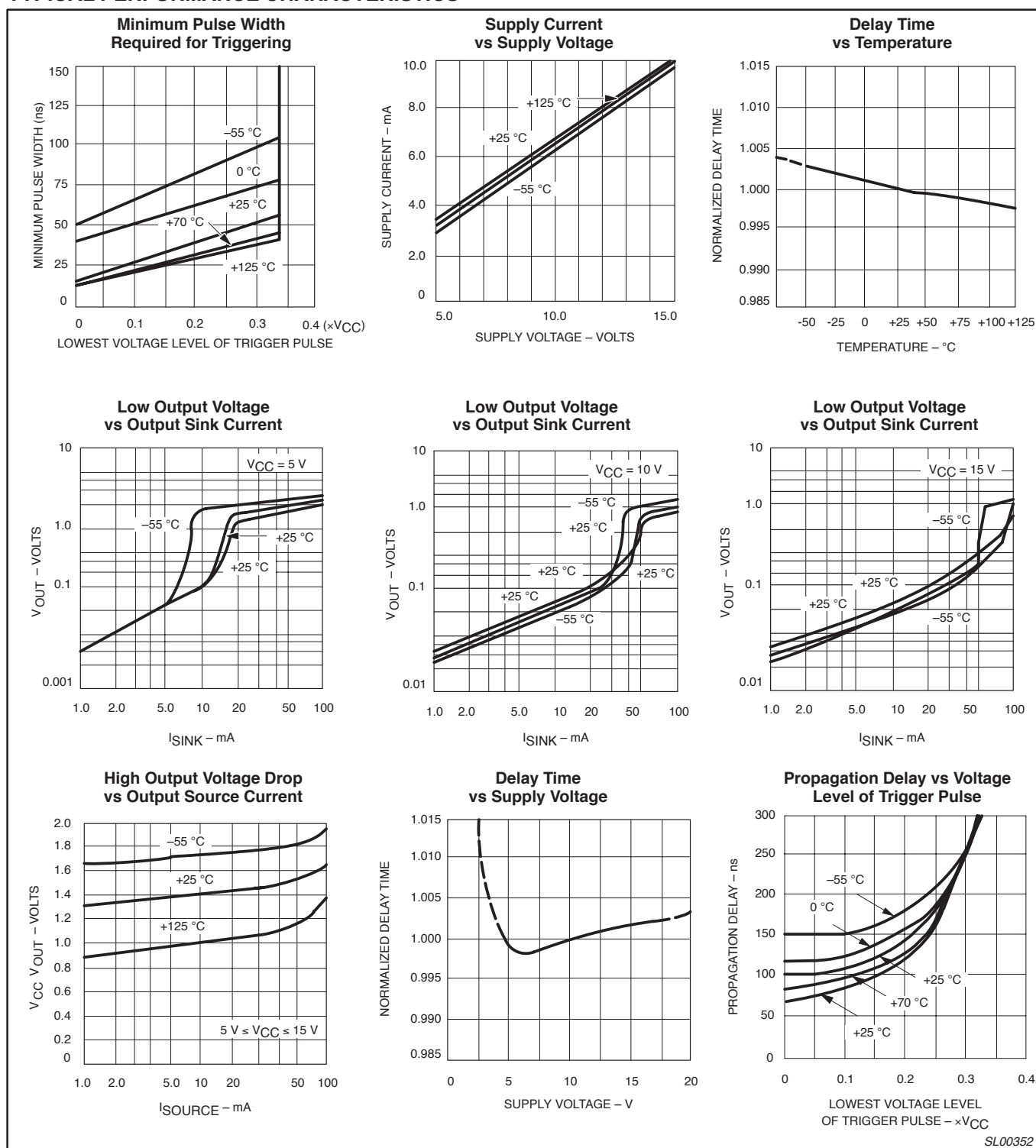


Figure 4. Typical Performance Characteristics

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TYPICAL APPLICATIONS

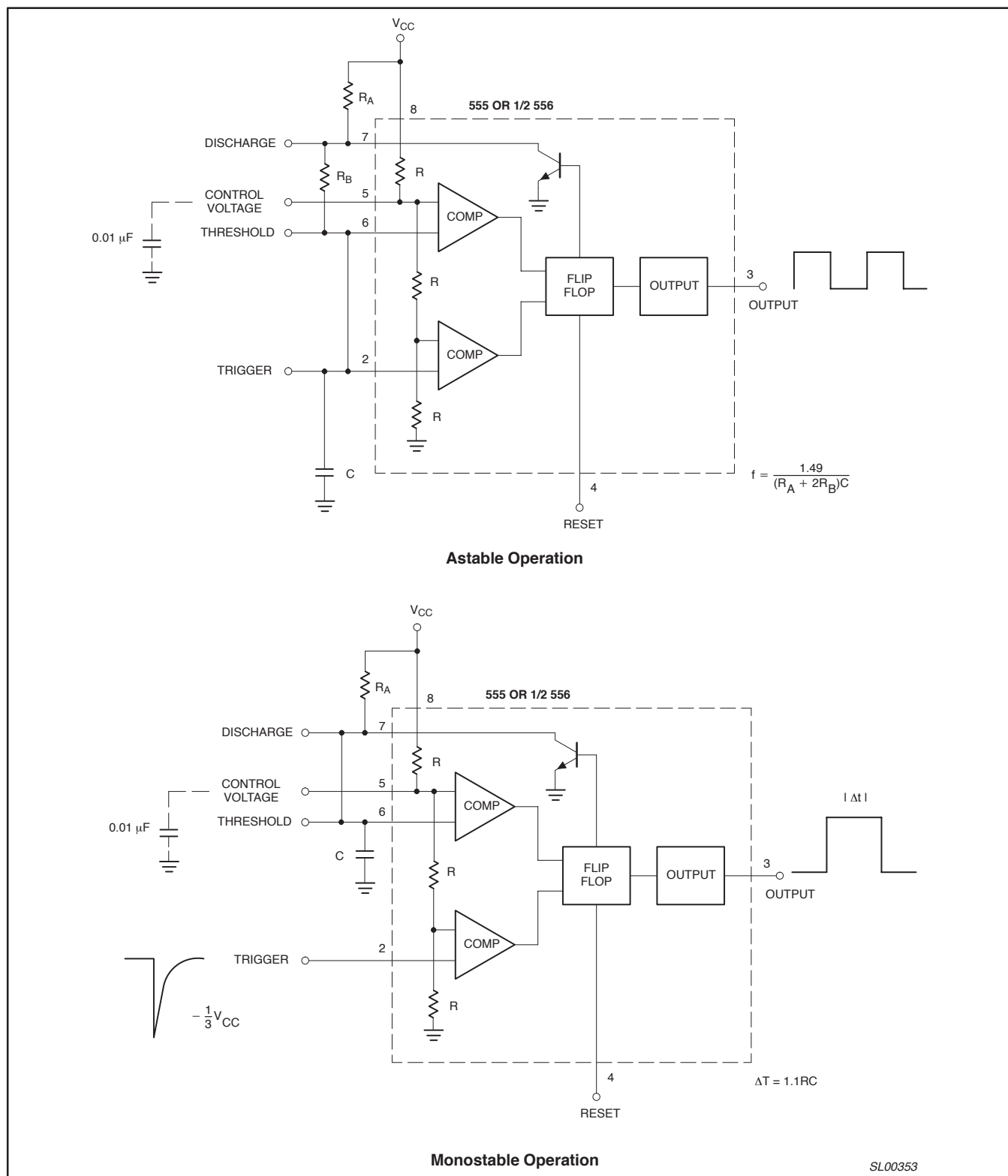


Figure 5. Typical Applications

SL00353

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TYPICAL APPLICATIONS

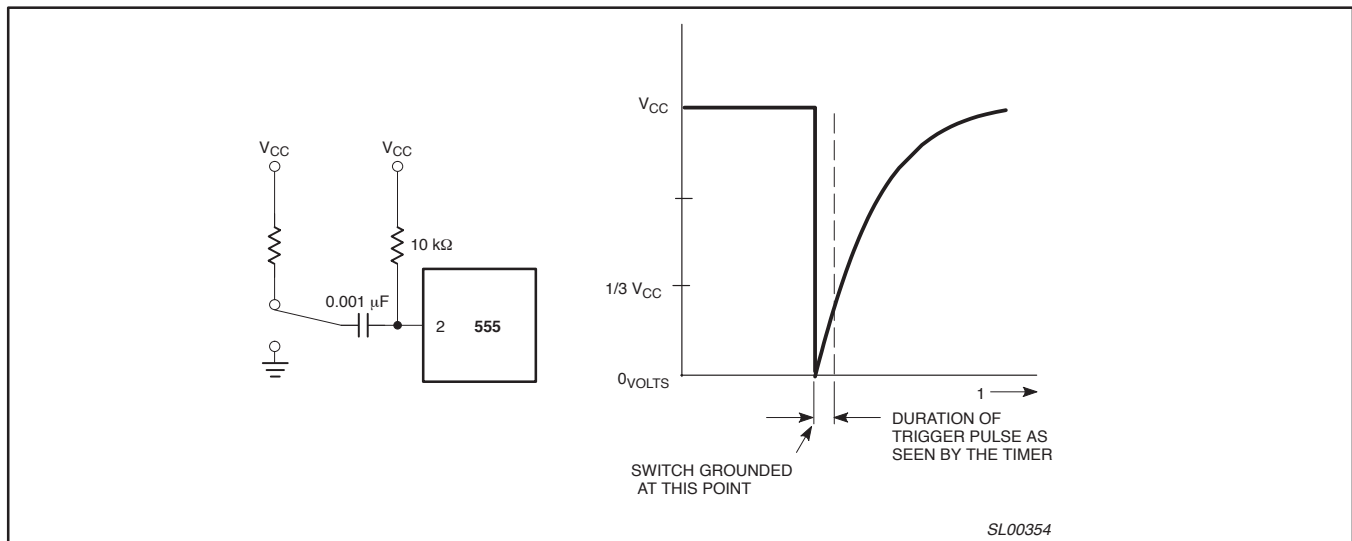


Figure 6. AC Coupling of the Trigger Pulse

Trigger Pulse Width Requirements and Time Delays

Due to the nature of the trigger circuitry, the timer will trigger on the negative going edge of the input pulse. For the device to time out properly, it is necessary that the trigger voltage level be returned to some voltage greater than one third of the supply before the time out period. This can be achieved by making either the trigger pulse sufficiently short or by AC coupling into the trigger. By AC coupling the trigger, see Figure 6, a short negative going pulse is achieved when the trigger signal goes to ground. AC coupling is most frequently used in conjunction with a switch or a signal that goes to ground which initiates the timing cycle. Should the trigger be held low, without AC coupling, for a longer duration than the timing cycle the output will remain in a high state for the duration of the low trigger signal, without regard to the threshold comparator state. This is due to the predominance of Q_{15} on the base of Q_{16} , controlling the state of the bi-stable flip-flop. When the trigger signal then returns to a high level, the output will fall immediately. Thus, the output signal will follow the trigger signal in this case.

Another consideration is the "turn-off time". This is the measurement of the amount of time required after the threshold reaches $2/3 V_{CC}$ to turn the output low. To explain further, Q_1 at the threshold input turns on after reaching $2/3 V_{CC}$, which then turns on Q_5 , which turns on Q_6 . Current from Q_6 turns on Q_{16} which turns Q_{17} off. This allows current from Q_{19} to turn on Q_{20} and Q_{24} to give an output low. These steps cause the 2 μs max. delay as stated in the data sheet.

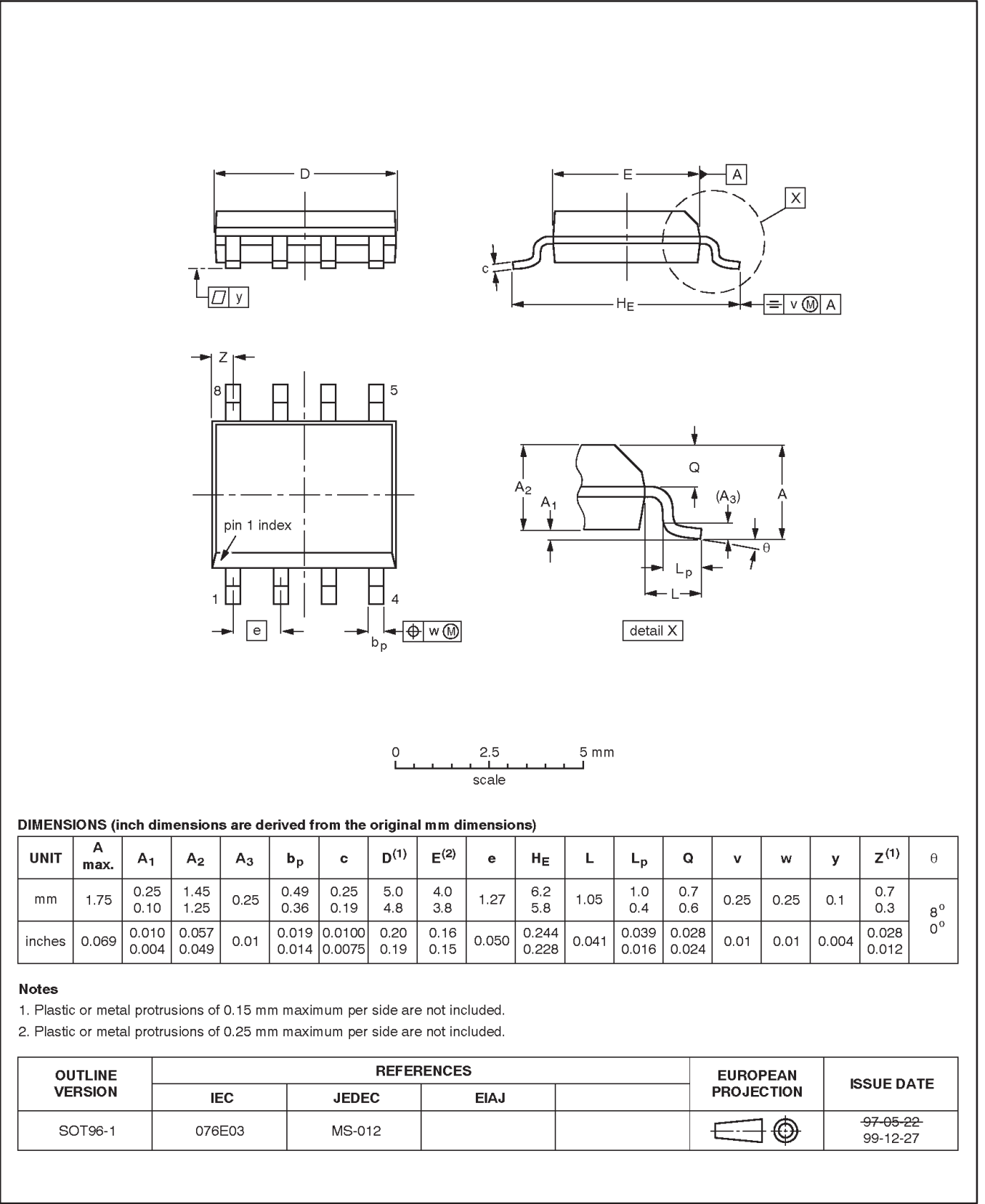
Also, a delay comparable to the turn-off time is the trigger release time. When the trigger is low, Q_{10} is on and turns on Q_{11} which turns on Q_{15} . Q_{15} turns off Q_{16} and allows Q_{17} to turn on. This turns off current to Q_{20} and Q_{24} , which results in output high. When the trigger is released, Q_{10} and Q_{11} shut off, Q_{15} turns off, Q_{16} turns on and the circuit then follows the same path and time delay explained as "turn off time". This trigger release time is very important in designing the trigger pulse width so as not to interfere with the output signal as explained previously.

Timer

NE/SA/SE555/SE555C

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

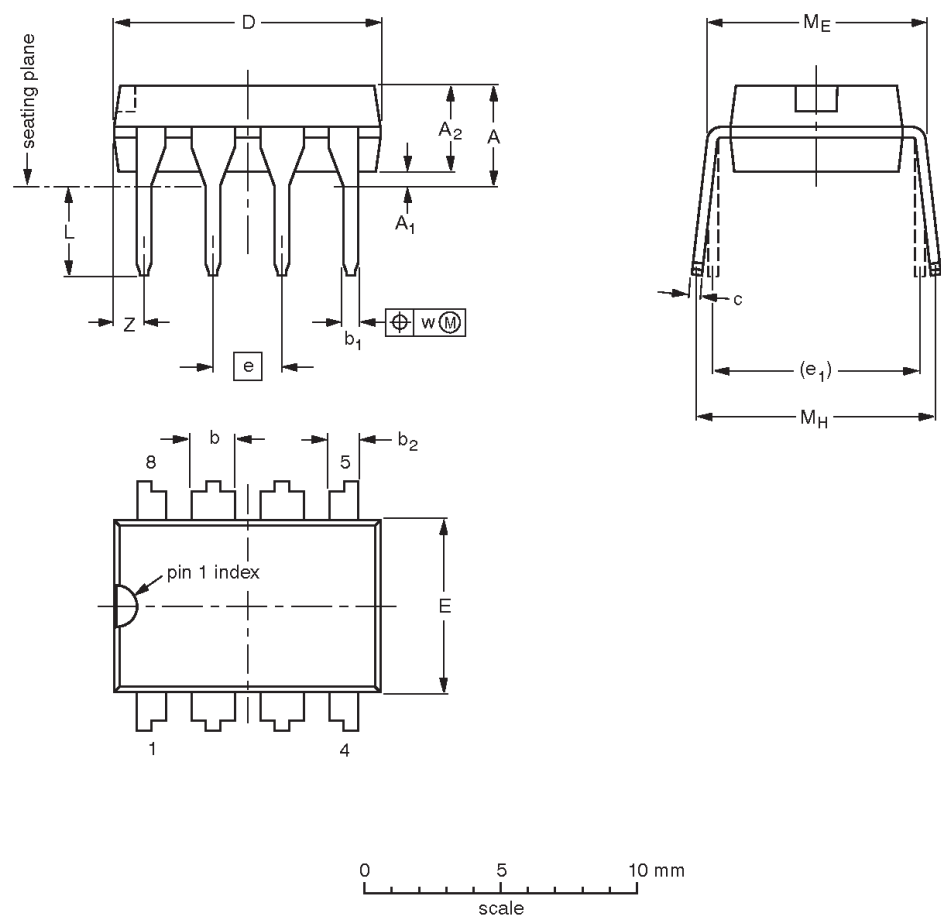


Timer

NE/SA/SE555/SE555C

DIP8: plastic dual in-line package; 8 leads (300 mil)

SOT97-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	b ₂	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT97-1	050G01	MO-001	SC-504-8			95-02-04 99-12-27

Timer

NE/SA/SE555/SE555C

REVISION HISTORY

Rev	Date	Description
2	20030214	Product data (9397 750 11129); ECN 853-0036 29156 of 06 November 2002. Supersedes Product specification dated August 31, 1994. Modifications: • Remove all cerdip information from the data sheet. Package type discontinued. • 'Absolute maximum ratings' table: T{SOLD} rating changed from '+300 °C' to '+230 °C'.
	19940831	Product specification; ECN 853-0036 13721 of 31 August 1994. (Filename = NE_SA555X.pdf)

Timer

NE/SA/SE555/SE555C

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I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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