AN 16.16

Configuration to Enable USB251x XNOR_MODE

1 Overview

The USB251x has an internal controller which is used to enable an XNOR_MODE that an OEM can utilize to check continuity of the I/O pins.

A “0” result will come out if all input pins in the XNOR chain are “0”, or if an even number of input pins have a "1" asserted.

A “1” result will come out if all input pins in the XNOR chain are “0” except for one, which is a “1”, or if an odd number of pins have a '1' asserted. The OEM can toggle one pin at a time and check the change in polarity of the XNOR output pin.

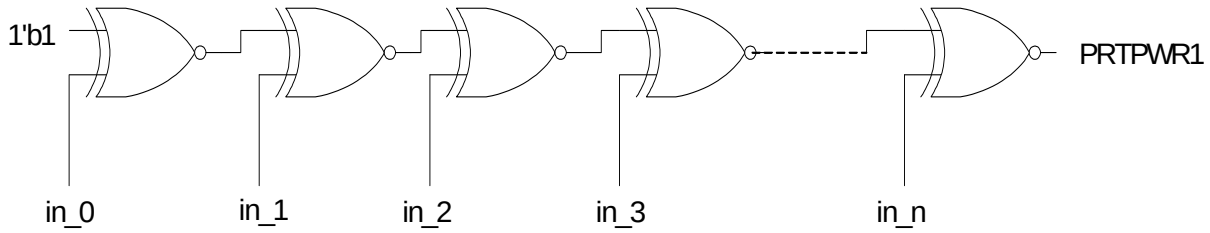

Figure 1.1 XNOR Chain Diagram

2 Audience

This application note assumes that the reader is familiar with hardware design, USB protocols, and USB hubs. The goal of the application note is to provide information on using XNOR_MODE.

3 XNOR_MODE Controller

The XNOR_MODE controller has a serial interface. When a serial data string is shifted into the controller, it recognizes the data pattern and enables XNOR_MODE.

4 XNOR_MODE Description

When XNOR_MODE is enabled, the normal functions are disconnected from each device pin, and all pins (except Power, Ground, XTAL1, XTAL2, RBIAS, REG_EN, RESET_N, and PRTPWR1) are connected internally to an XNOR chain as inputs. The PRTPWR1 pin is the XNOR output.

The XNOR_MODE test mode also disables the clocks by not feeding the crystal clock or the oscillator clock.

Note 4.1 USB2513 and USB2514: XNOR_MODE will work as specified.

Note 4.2 XNOR test mode is not supported in the USB2512.

Note 4.3 If using a device with disabled (and therefore unimplemented) ports, the pins for the disabled port are still in the XNOR chain and accounted for appropriately.

5 Configuration

1. After the device is powered up, wait until the device's PLL is stable.
2. Drive the TEST pin to "high."
3. Wait for a number of clock cycles (>10) on the SCL pin.
4. Drive the OCS1_N pin to "low" on the next falling edge of the SCL pin.
5. After the falling edge of the OCS1_N pin, wait 2 clock cycles until the third falling edge of the clock on the SCL pin.
6. Drive the data pattern 8'b 00000001 onto the SDA pin at every falling edge of the clock on the SCL pin.
7. Wait for 4 clock cycles on the SCL pin.
8. At the next falling edge of the clock cycle, drive the data pattern 16'b 0000000000000001 onto the SDA pin at every falling edge of the clock on the SCL pin.
9. Wait for 5 clock cycles.
10. XNOR_MODE is now enabled.
11. Exit XNOR_MODE by performing a hardware reset.

6 Serial Interface Technical Characteristics

- Present the data on the falling edge of the clock.
- The USB251x reads data on next rising edge.

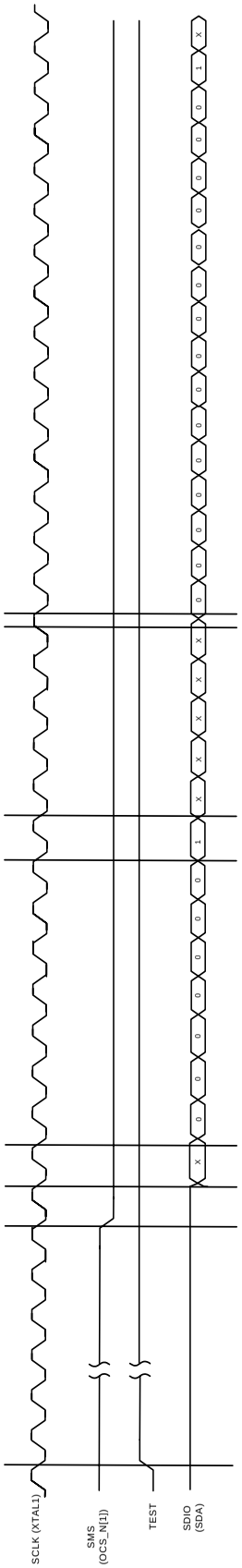

Figure 6.1 Timing Diagram

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