

DATA SHEET

PDTC144E series

NPN resistor-equipped transistors;

$R1 = 47\text{ k}\Omega$, $R2 = 47\text{ k}\Omega$

Product data sheet
Supersedes data of 2004 Mar 23

2004 Aug 17

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PDTC144E series

FEATURES

- Built-in bias resistors
- Simplified circuit design
- Reduction of component count
- Reduced pick and place costs.

APPLICATIONS

- General purpose switching and amplification
- Inverter and interface circuits
- Circuit driver.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V _{CEO}	collector-emitter voltage	–	50	V
I _O	output current (DC)	–	100	mA
R1	bias resistor	47	–	k Ω
R2	bias resistor	47	–	k Ω

DESCRIPTION

NPN resistor-equipped transistor (see “Simplified outline, symbol and pinning” for package details).

PRODUCT OVERVIEW

TYPE NUMBER	PACKAGE		MARKING CODE	PNP COMPLEMENT
	PHILIPS	EIAJ		
PDTC144EE	SOT416	SC-75	08	PDTA144EE
PDTC144EEF	SOT490	SC-89	08	PDTA144EEF
PDTC144EK	SOT346	SC-59	08	PDTA144EK
PDTC144EM	SOT883	SC-101	E7	PDTA144EM
PDTC144ES	SOT54 (TO-92)	SC-43	TC144E	PDTA144ES
PDTC144ET	SOT23	–	*08 ⁽¹⁾	PDTA144ET
PDTC144EU	SOT323	SC-70	*08 ⁽¹⁾	PDTA144EU

Note

- * = p: Made in Hong Kong.
* = t: Made in Malaysia.
* = W: Made in China.

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R1 = 47 kΩ, R2 = 47 kΩ

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SIMPLIFIED OUTLINE, SYMBOL AND PINNING

TYPE NUMBER	SIMPLIFIED OUTLINE AND SYMBOL	PINNING	
		PIN	DESCRIPTION
PDTC144ES	MAM364	1 2 3	base collector emitter
PDTC144EE PDTC144EEF PDTC144EK PDTC144ET PDTC144EU	Top view MDB269	1 2 3	base emitter collector
PDTC144EM	bottom view MHC506	1 2 3	base emitter collector

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ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PDTC144EE	–	plastic surface mounted package; 3 leads	SOT416
PDTC144EEF	–	plastic surface mounted package; 3 leads	SOT490
PDTC144EK	–	plastic surface mounted package; 3 leads	SOT346
PDTC144EM	–	leadless ultra small plastic package; 3 solder lands; body 1.0 × 0.6 × 0.5 mm	SOT883
PDTC144ES	–	plastic single-ended leaded (through hole) package; 3 leads	SOT54
PDTC144ET	–	plastic surface mounted package; 3 leads	SOT23
PDTC144EU	–	plastic surface mounted package; 3 leads	SOT323

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CBO}	collector-base voltage	open emitter	–	50	V
V _{CEO}	collector-emitter voltage	open base	–	50	V
V _{EBO}	emitter-base voltage	open collector	–	10	V
V _I	input voltage				
	positive		–	+40	V
	negative		–	–10	V
I _O	output current (DC)		–	100	mA
I _{CM}	peak collector current		–	100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C			
	SOT54	note 1	–	500	mW
	SOT23	note 1	–	250	mW
	SOT346	note 1	–	250	mW
	SOT323	note 1	–	200	mW
	SOT416	note 1	–	150	mW
	SOT490	notes 1 and 2	–	250	mW
	SOT883	notes 2 and 3	–	250	mW
T _{stg}	storage temperature		–65	+150	°C
T _j	junction temperature		–	150	°C
T _{amb}	operating ambient temperature		–65	+150	°C

Notes

1. Refer to standard mounting conditions.
2. Reflow soldering is the only recommended soldering method.
3. Refer to SOT883 standard mounting conditions; FR4 with 60 μ m copper strip line.

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th(j-a)}	thermal resistance from junction to ambient	in free air		
	SOT54	note 1	250	K/W
	SOT23	note 1	500	K/W
	SOT346	note 1	500	K/W
	SOT323	note 1	625	K/W
	SOT416	note 1	833	K/W
	SOT490	notes 1 and 2	500	K/W
	SOT883	notes 2 and 3	500	K/W

Notes

1. Refer to standard mounting conditions.
2. Reflow soldering is the only recommended soldering method.
3. Refer to SOT883 standard mounting conditions; FR4 with 60 μ m copper strip line.

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I _{CBO}	collector-base cut-off current	V _{CB} = 50 V; I _E = 0 A	–	–	100	nA
I _{CEO}	collector-emitter cut-off current	V _{CE} = 30 V; I _B = 0 A	–	–	1	μ A
		V _{CE} = 30 V; I _B = 0 A; T _j = 150 °C	–	–	50	μ A
I _{EBO}	emitter-base cut-off current	V _{EB} = 5 V; I _C = 0 A	–	–	90	μ A
h _{FE}	DC current gain	V _{CE} = 5 V; I _C = 5 mA	80	–	–	
V _{CEsat}	collector-emitter saturation voltage	I _C = 10 mA; I _B = 0.5 mA	–	–	150	mV
V _{i(off)}	input-off voltage	I _C = 100 μ A; V _{CE} = 5 V	–	1.2	0.8	V
V _{i(on)}	input-on voltage	I _C = 2 mA; V _{CE} = 0.3 V	3	1.6	–	V
R1	input resistor		33	47	61	k Ω
$\frac{R2}{R1}$	resistor ratio		0.8	1	1.2	
C _c	collector capacitance	I _E = I _e = 0 A; V _{CB} = 10 V; f = 1 MHz	–	–	2.5	pF

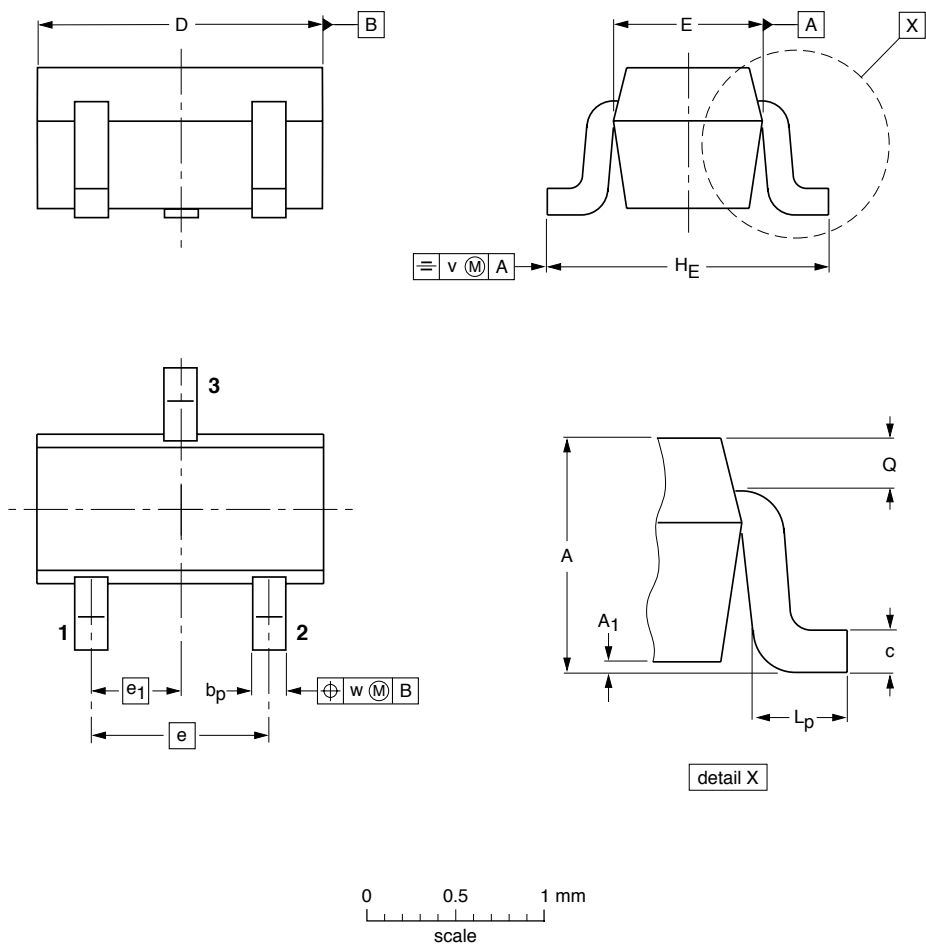
NPN resistor-equipped transistors;
R1 = 47 kΩ, R2 = 47 kΩ

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PACKAGE OUTLINES

Plastic surface-mounted package; 3 leads

SOT416



DIMENSIONS (mm are the original dimensions)

UNIT	A	A1 max	bp	c	D	E	e	e1	HE	Lp	Q	v	w
mm	0.95 0.60	0.1	0.30 0.15	0.25 0.10	1.8 1.4	0.9 0.7	1	0.5	1.75 1.45	0.45 0.15	0.23 0.13	0.2	0.2

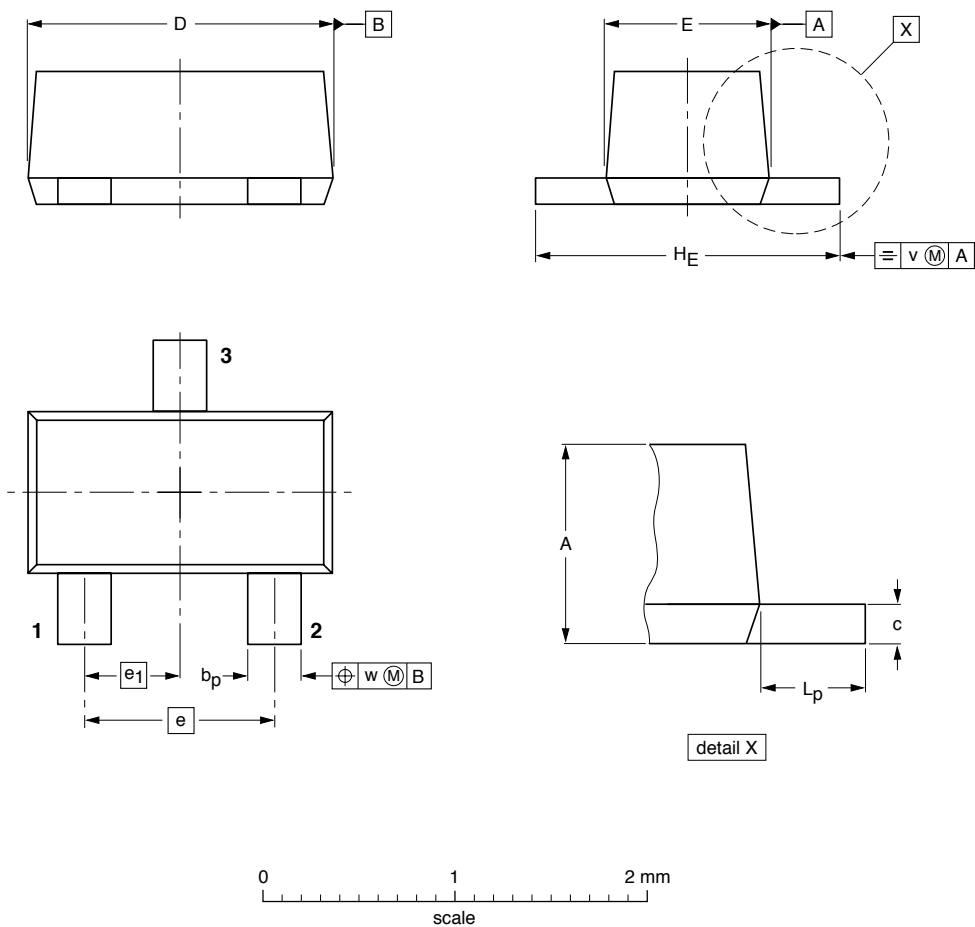
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	IEC	JEDEC	JEITA			
SOT416			SC-75			04-11-04 06-03-16

NPN resistor-equipped transistors;
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Plastic surface-mounted package; 3 leads

SOT490



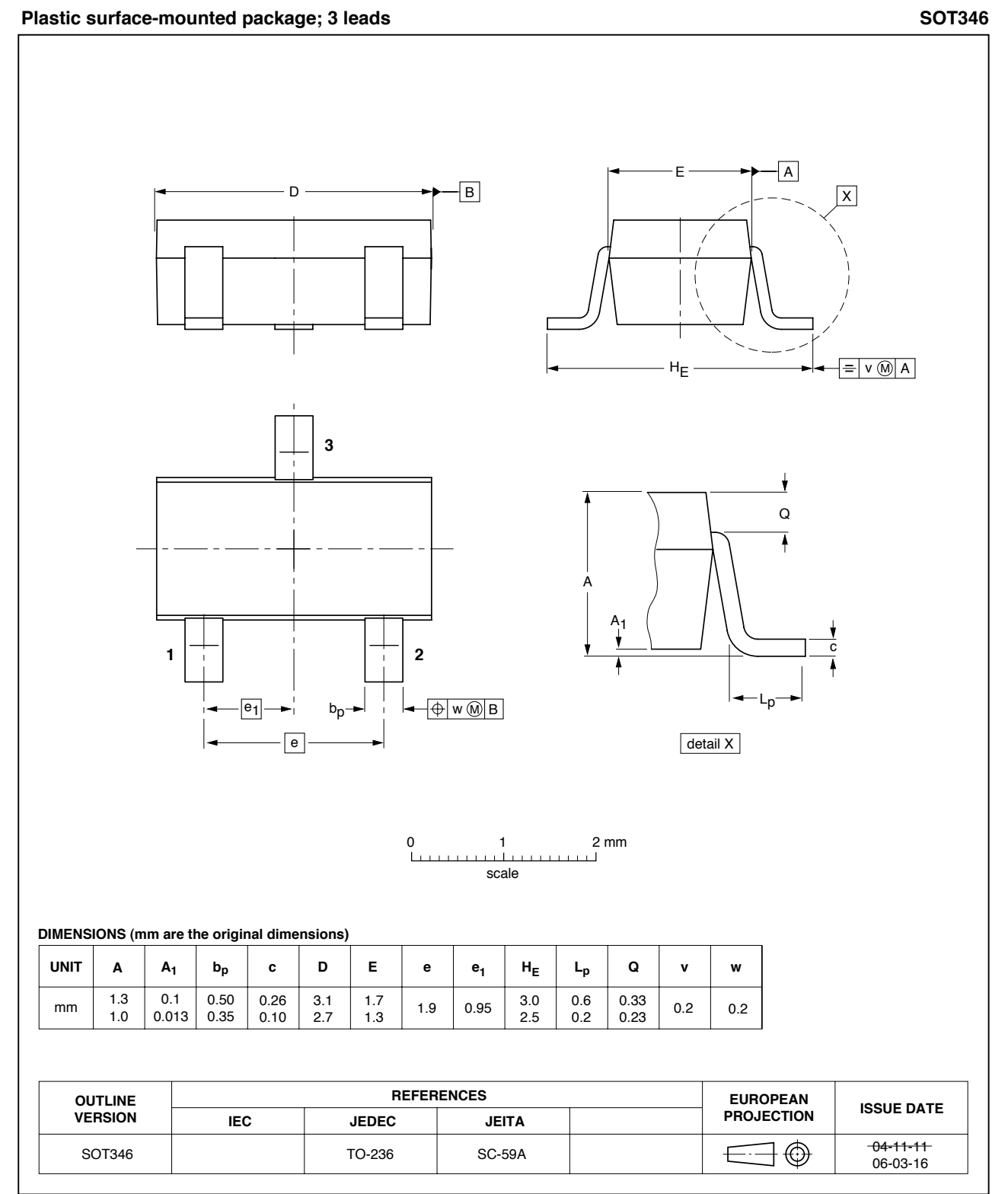
DIMENSIONS (mm are the original dimensions)

UNIT	A	b _p	c	D	E	e	e ₁	H _E	L _p	v	w
mm	0.8 0.6	0.33 0.23	0.2 0.1	1.7 1.5	0.95 0.75	1.0	0.5	1.7 1.5	0.5 0.3	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT490			SC-89			05-07-28 06-03-16

NPN resistor-equipped transistors;
R1 = 47 kΩ, R2 = 47 kΩ

PDTC144E series

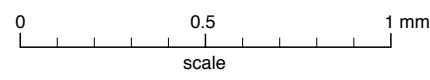
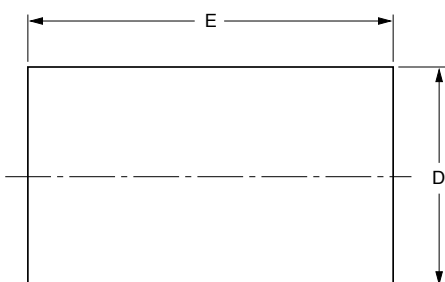
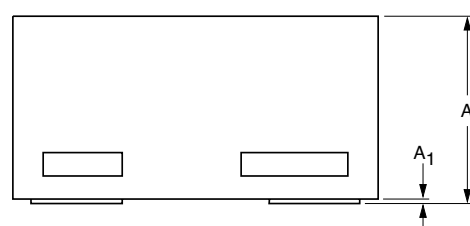
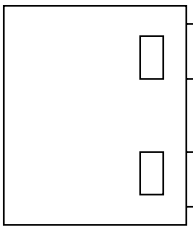
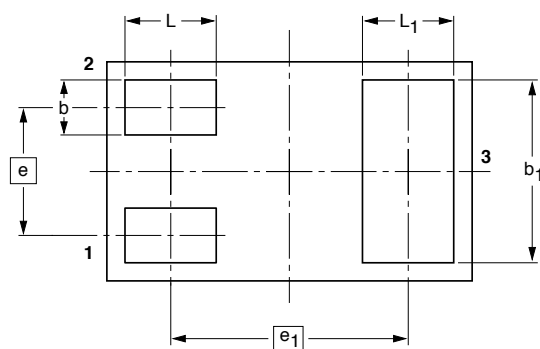


NPN resistor-equipped transistors;
R1 = 47 kΩ, R2 = 47 kΩ

PDTC144E series

Leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.5 mm

SOT883



DIMENSIONS (mm are the original dimensions)

UNIT	A ⁽¹⁾	A ₁ max.	b	b ₁	D	E	e	e ₁	L	L ₁
mm	0.50 0.46	0.03	0.20 0.12	0.55 0.47	0.62 0.55	1.02 0.95	0.35	0.65	0.30 0.22	0.30 0.22

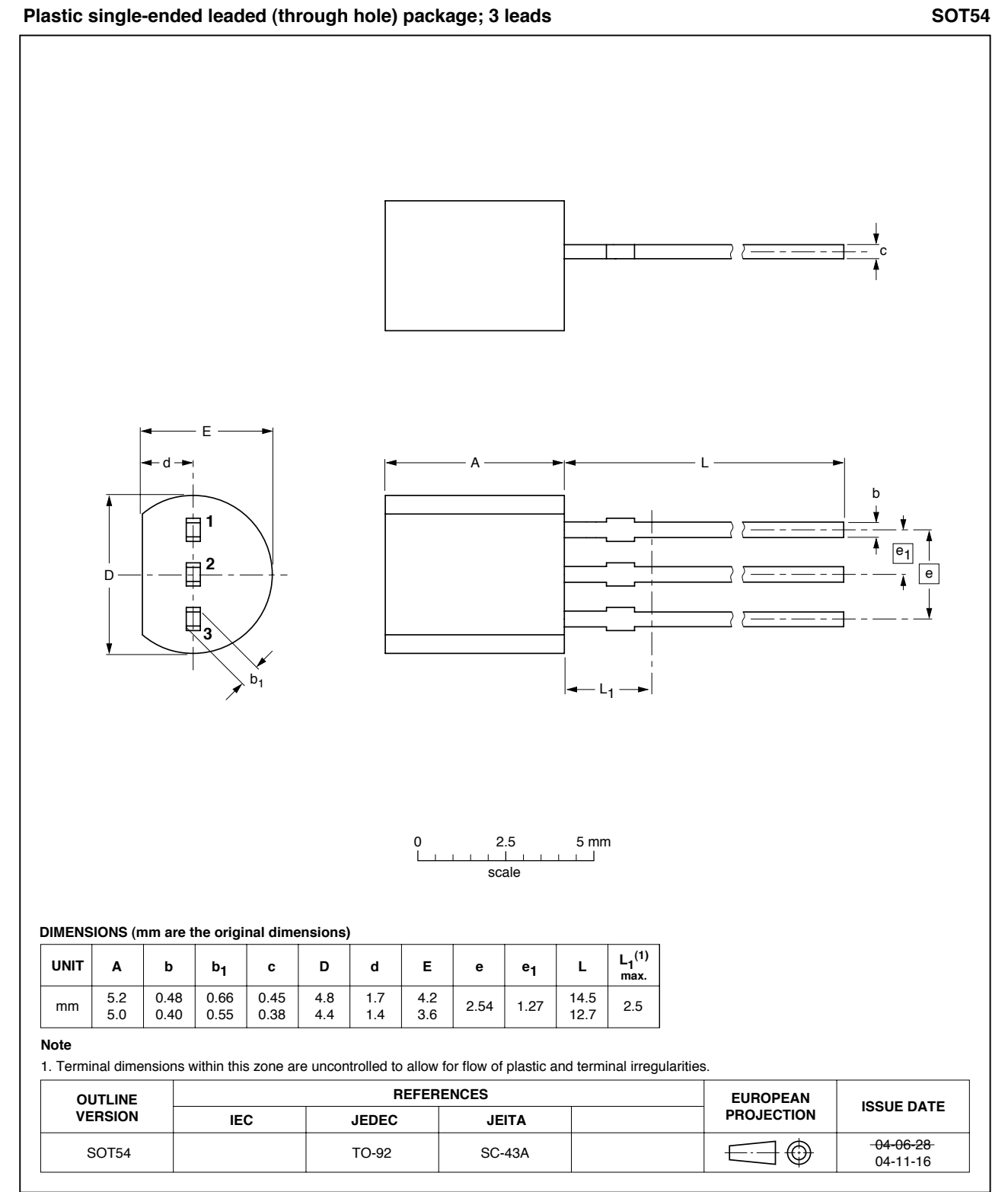
Note

1. Including plating thickness

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT883			SC-101			03-02-05 03-04-03

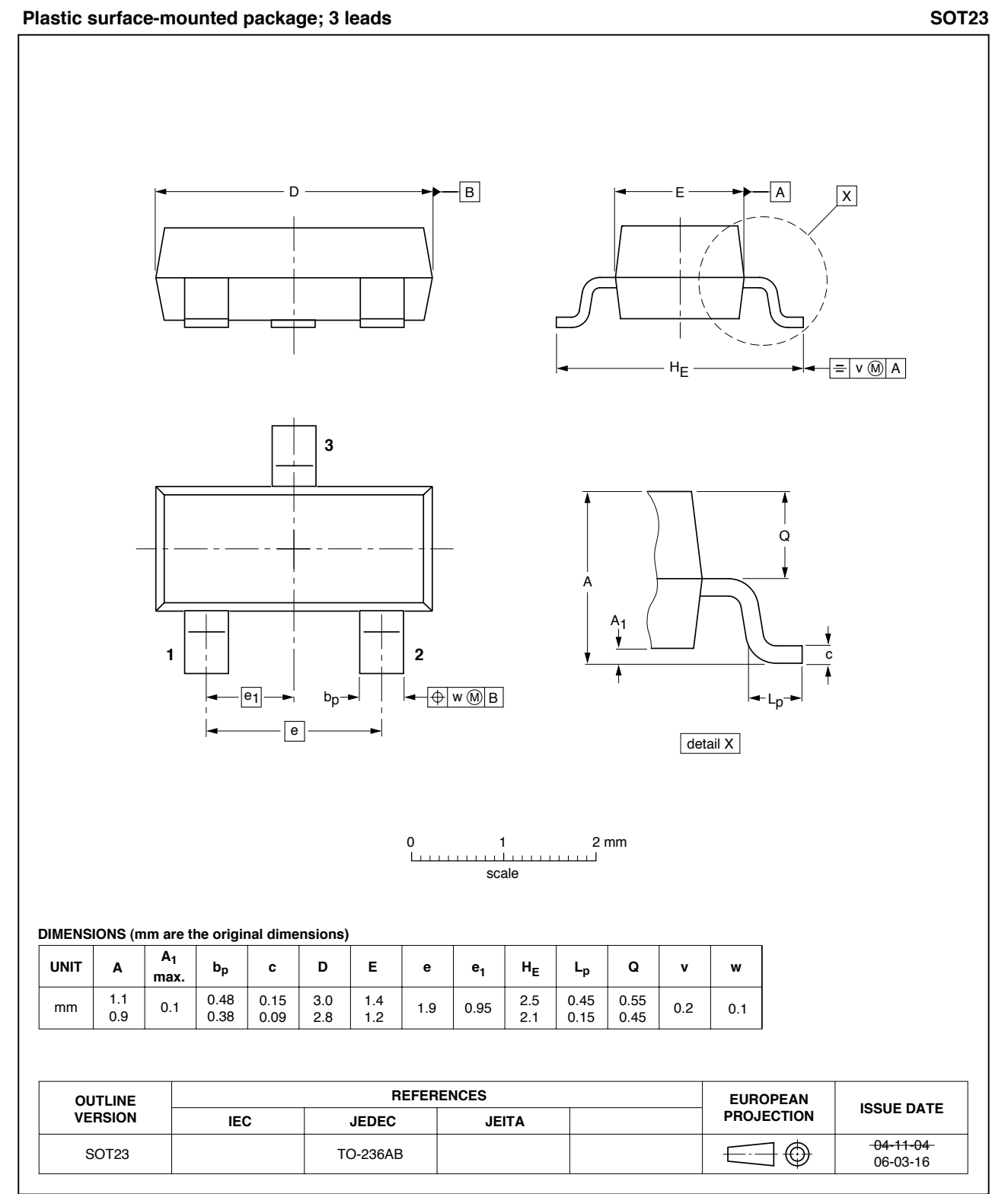
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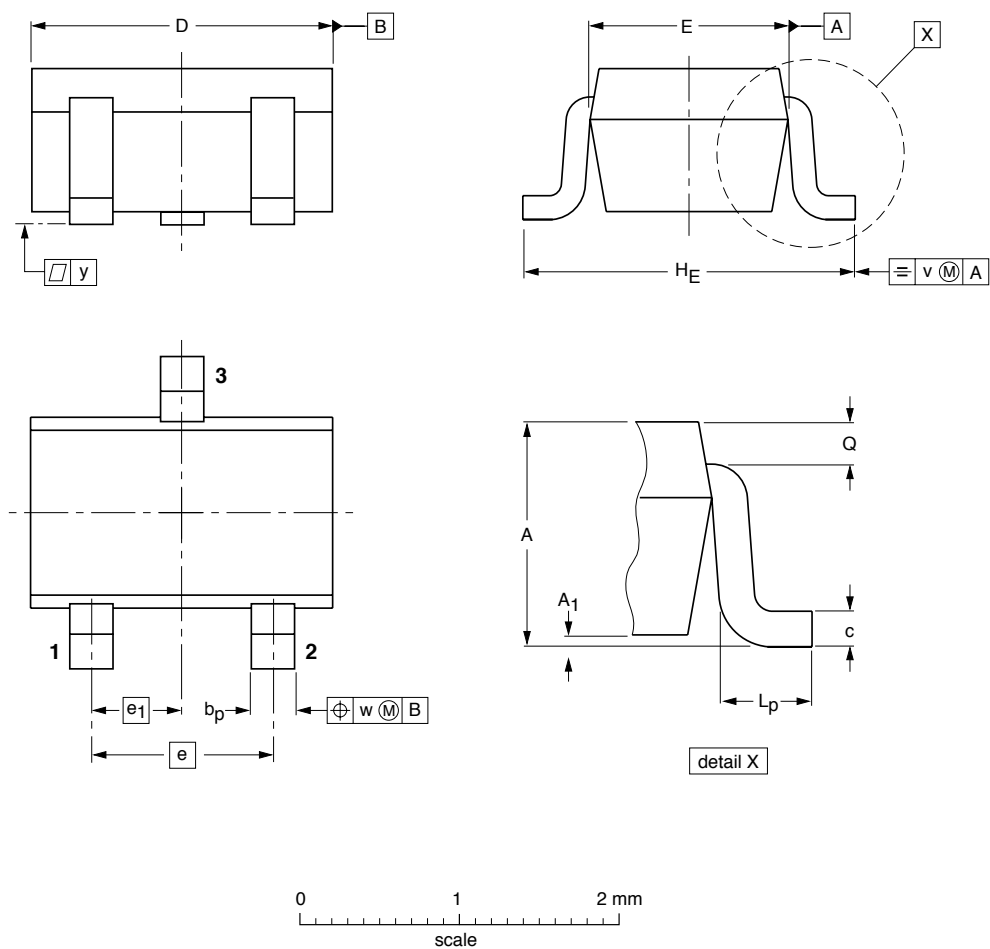


NPN resistor-equipped transistors;
R1 = 47 kΩ, R2 = 47 kΩ

PDTC144E series

Plastic surface-mounted package; 3 leads

SOT323



DIMENSIONS (mm are the original dimensions)

UNIT	A	A1 max	bp	c	D	E	e	e1	HE	Lp	Q	v	w
mm	1.1 0.8	0.1	0.4 0.3	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT323			SC-70			04-11-04 06-03-16

NPN resistor-equipped transistors;
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DATA SHEET STATUS

DOCUMENT STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

Notes

1. Please consult the most recently issued document before initiating or completing a design.
2. The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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Customer notification

This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content, except for package outline drawings which were updated to the latest version.

Contact information

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